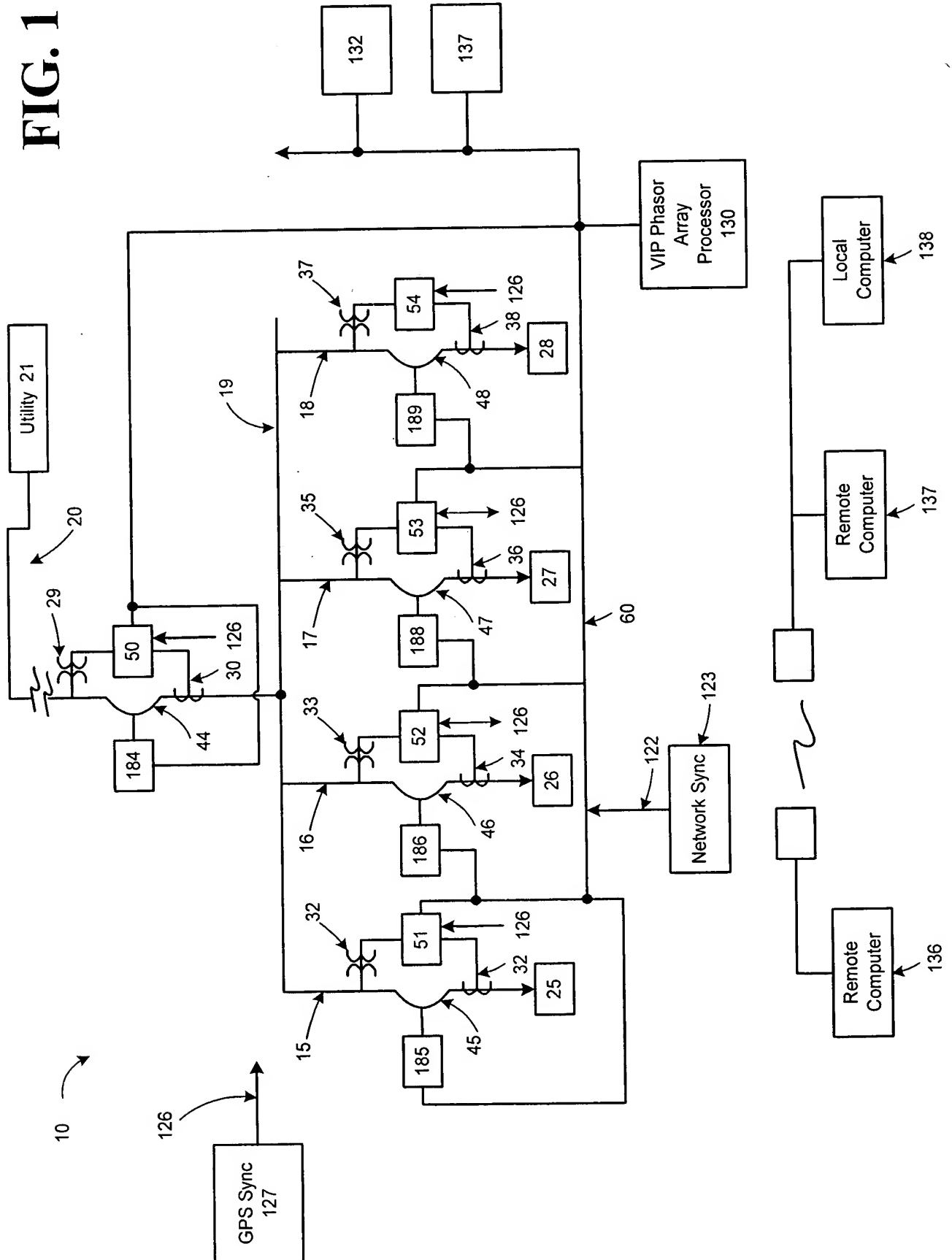




FIG. 1



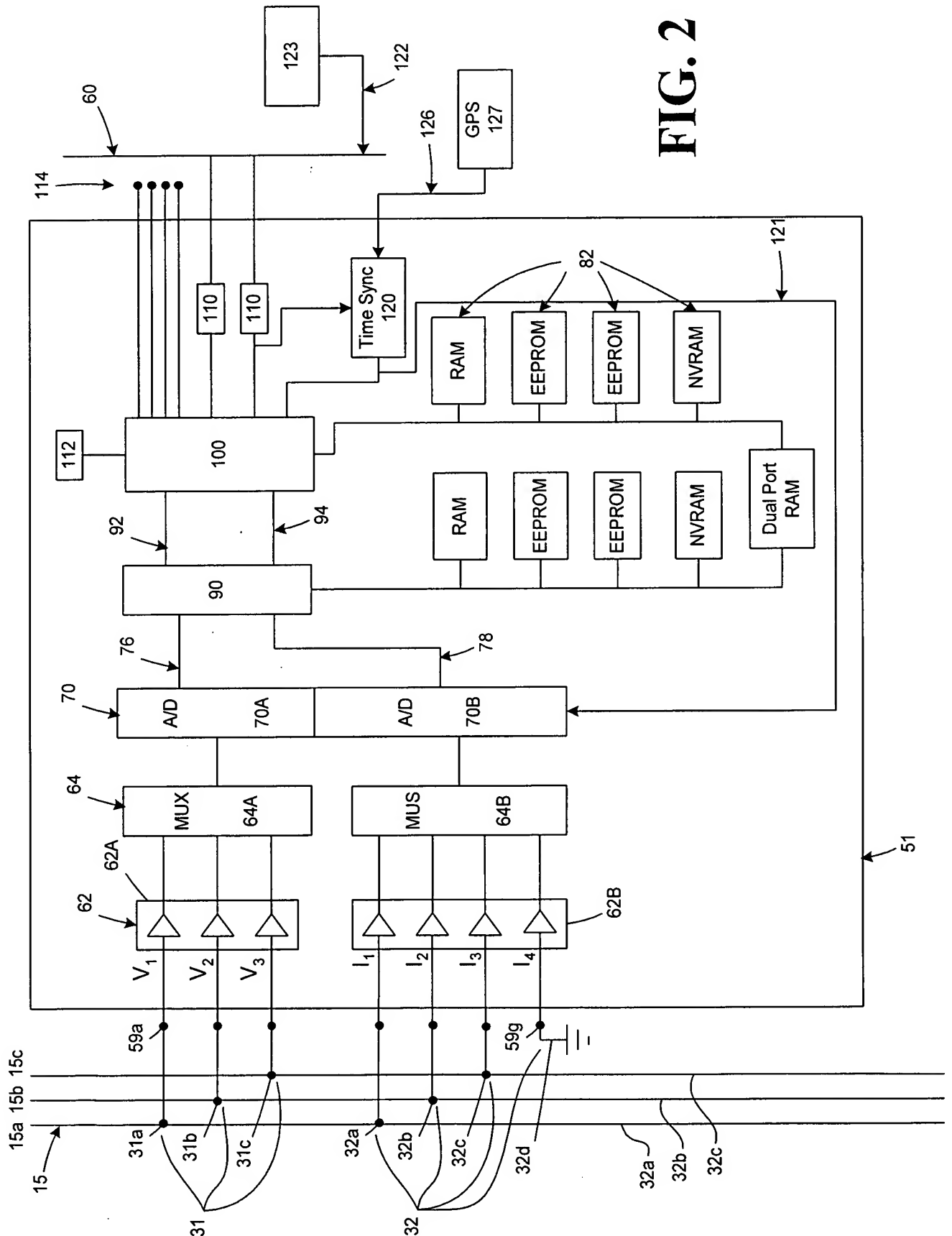
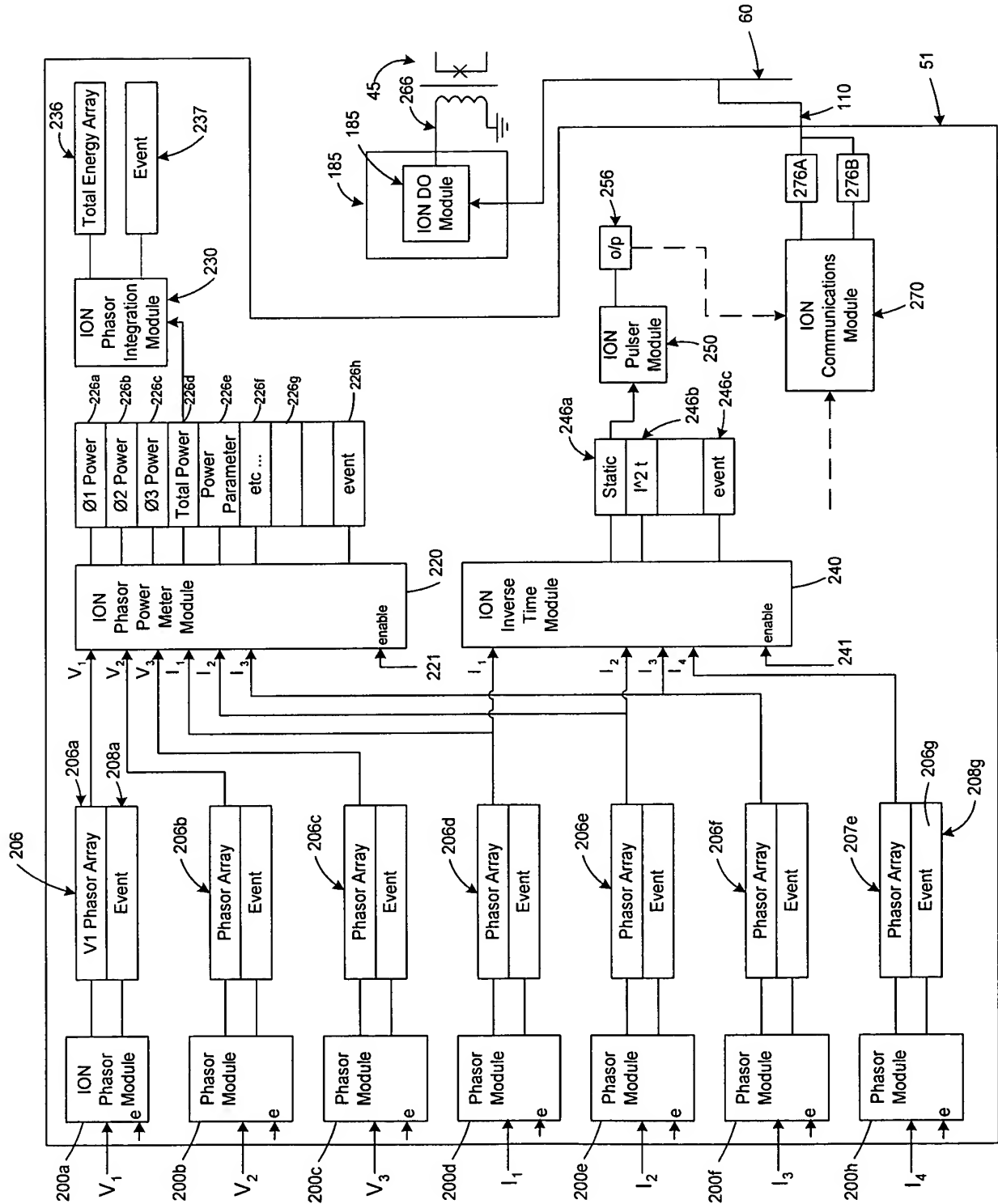


FIG. 2



Phasor ION Module Diagram

FIG. 3

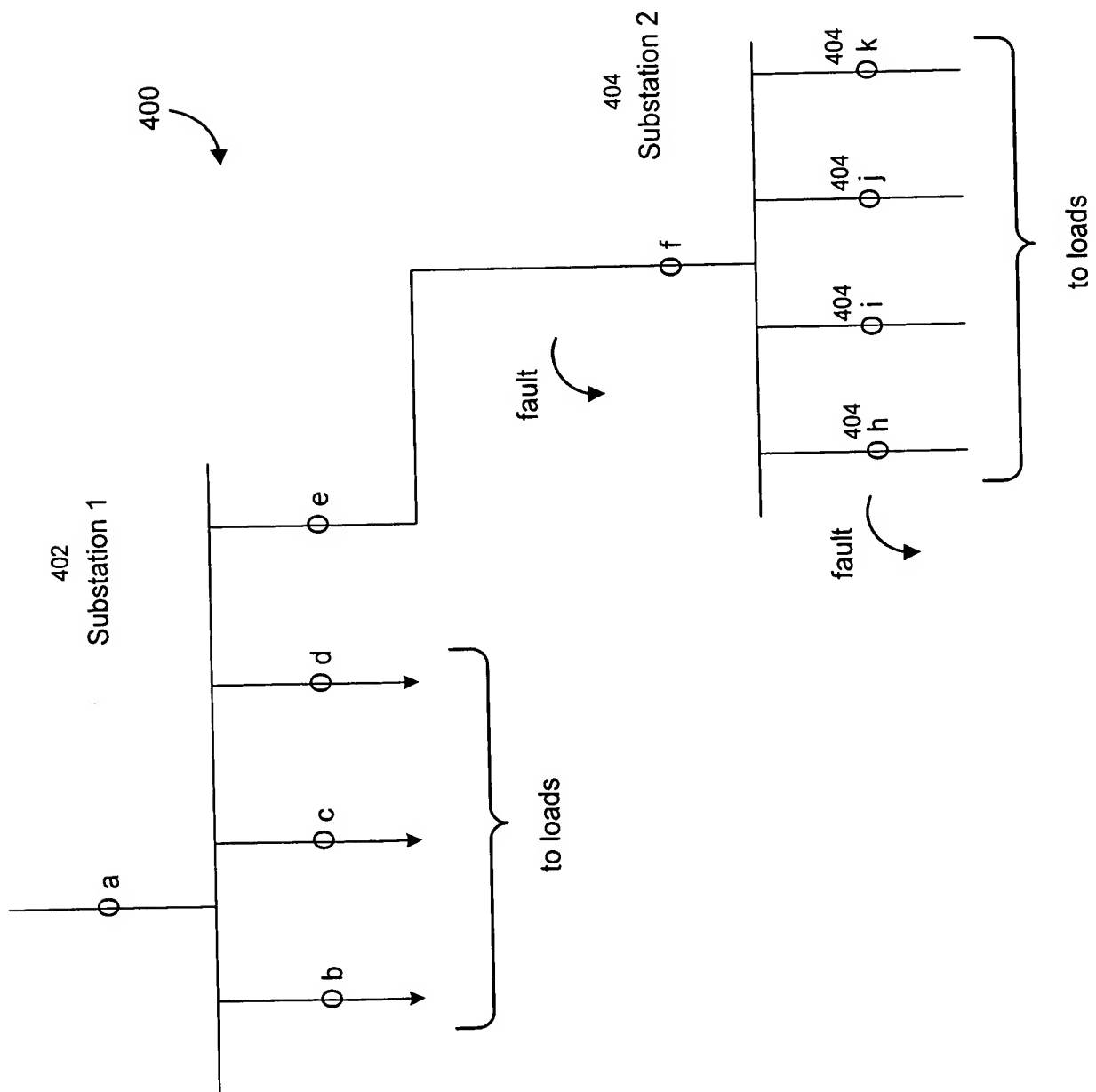


FIG. 5

FIG. 6

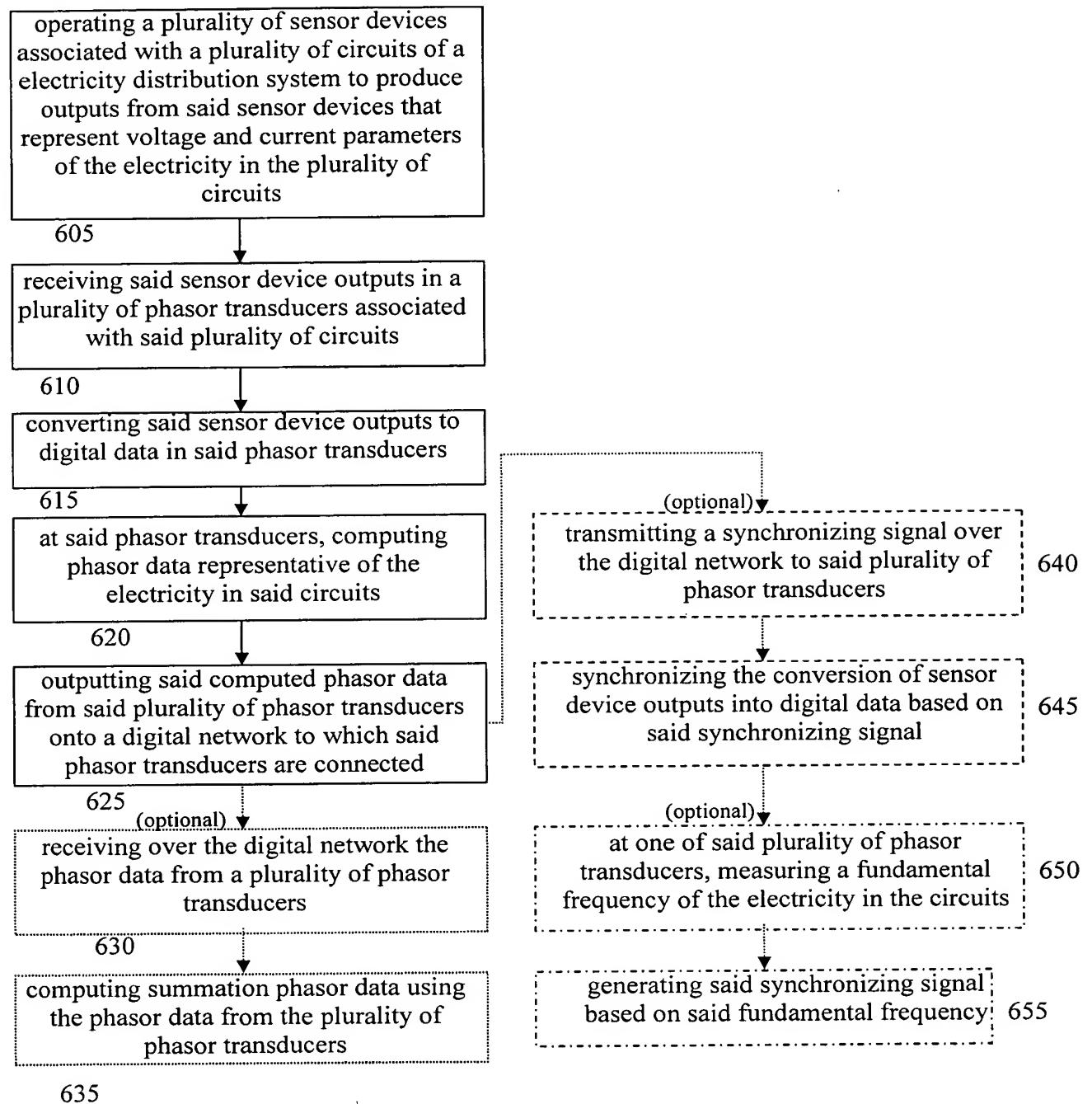


FIG. 7

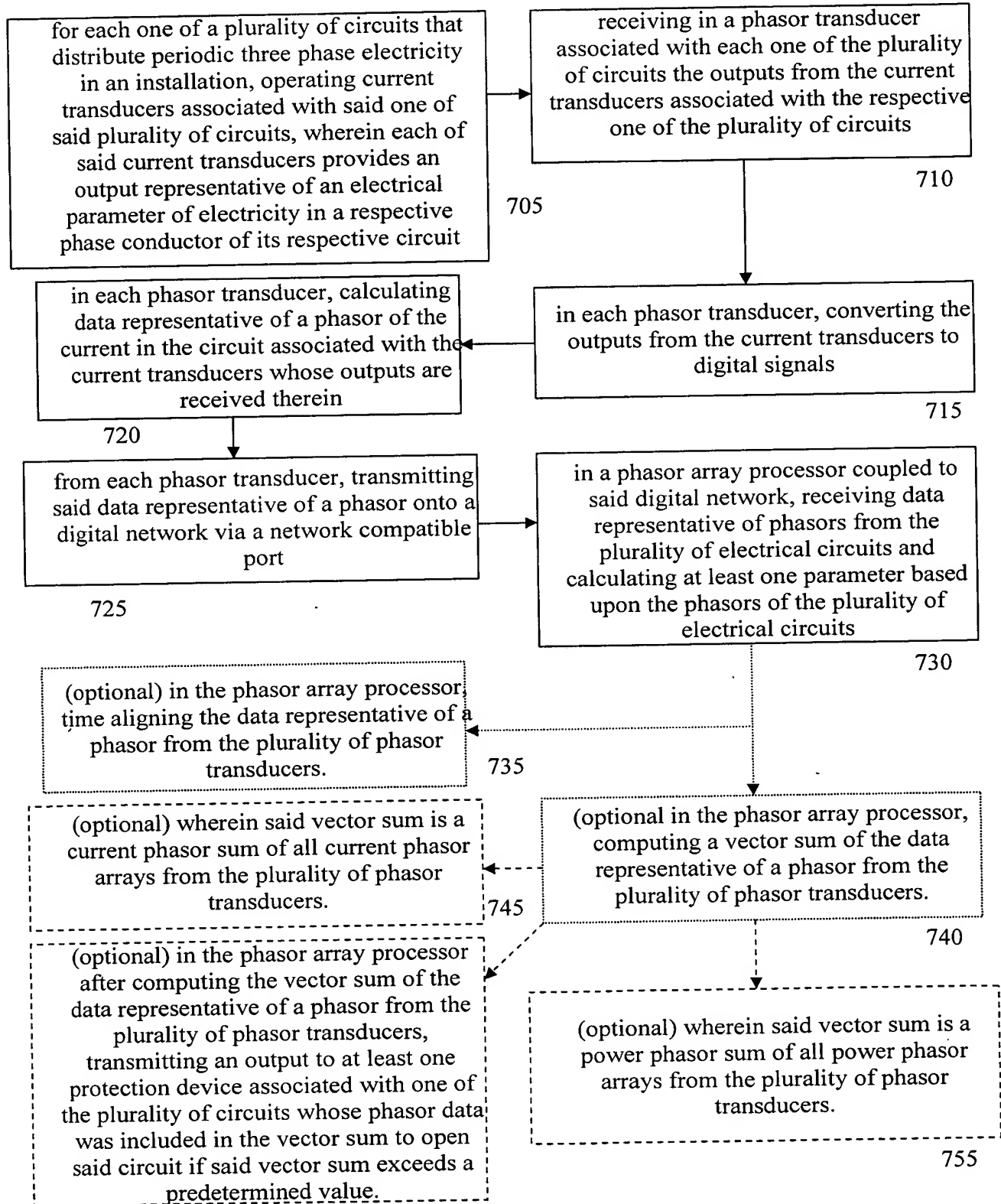


FIG. 8

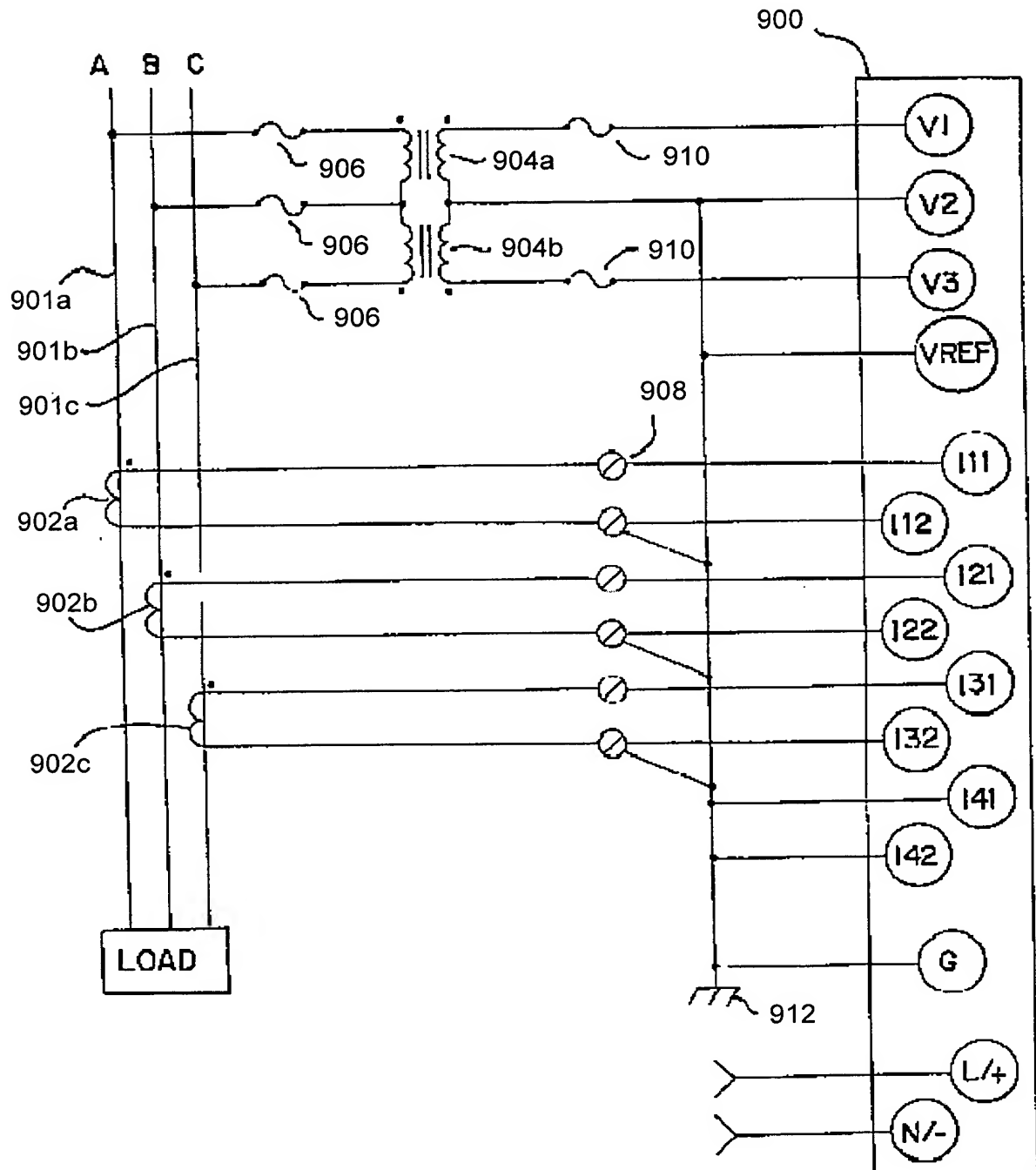


FIG. 9

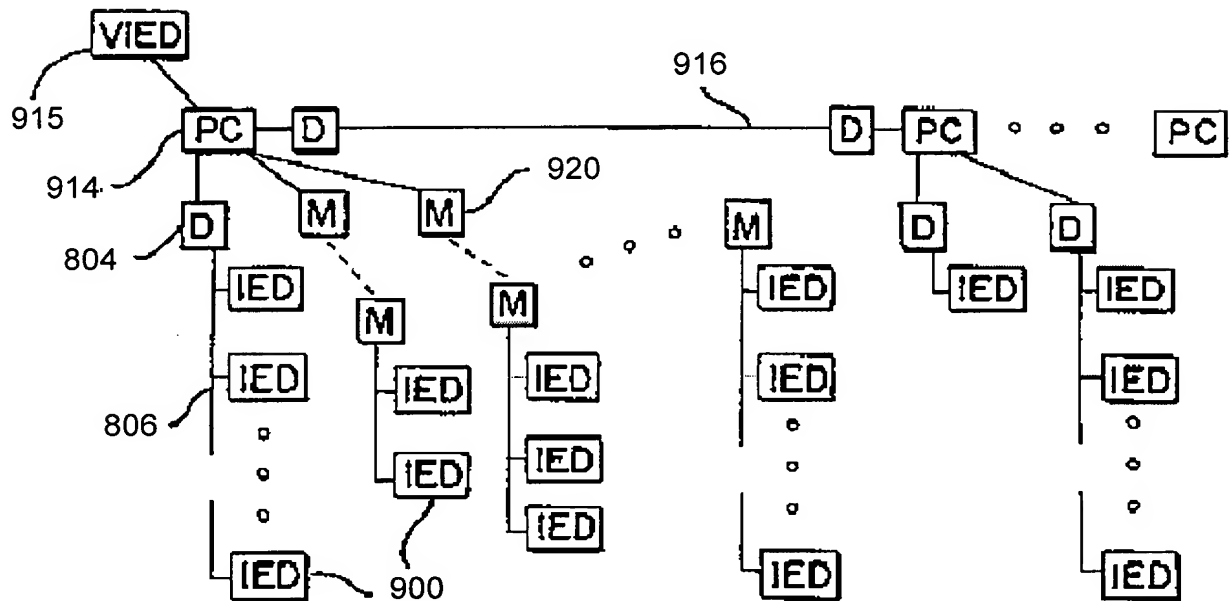


FIG. 11

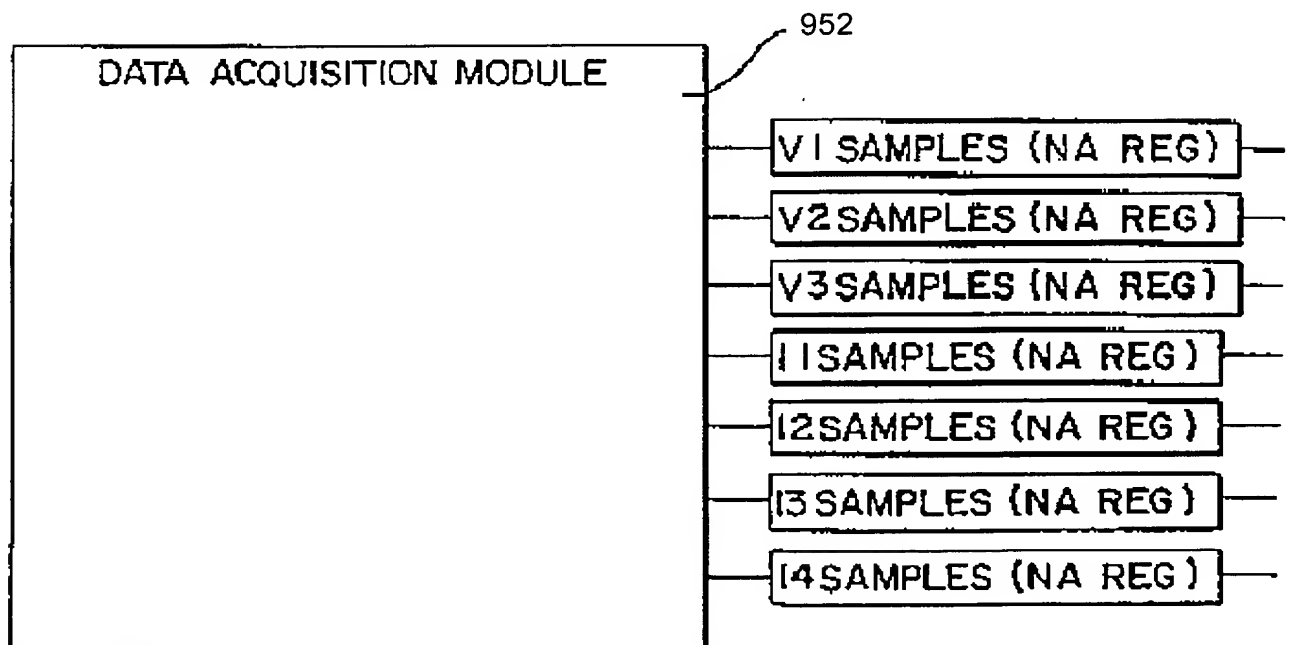


FIG. 10

The diagram illustrates a system architecture with three main components: an AUX BOARD (824), a CPU BOARD (846), and a MOTHERBOARD (825).

- AUX BOARD (824):** Contains four auxiliary input channels (AUX1, AUX2, AUX3, AUX4) and a CALIBRATION CONSTANTS EEPROM (820). It is connected to the CPU BOARD via a SIGNAL CONDITIONING CIRCUITRY (822).
- CPU BOARD (846):** The central processing unit, containing:
 - DSP BUS (832):** Connects to 32K BYTE RAM (PROGRAM) (826) and 32K BYTE RAM (DATA) (850).
 - Digital Signal Processor (DSP) (828):** Connected to the RAMs and a PORT RAM (827).
 - Digital Converters (A/D) (829, 830):** Receive signals from the MOTHERBOARD and output to the DSP.
 - A/D BUS (831):** Connects the digital converters to the DSP.
 - EEPROM (834):** Connected to a REAL TIME CLOCK (835) and a MICRO-CONTROLLER BUS (835).
 - 256K BYTE NON-VOLATILE RAM (833):** Connected to the MICRO-CONTROLLER BUS.
 - MICRO-CONTROLLER (835):** Manages system operations and is connected to the A/D SAMPLE CLOCK (842) and FUNDAMENTAL FREQUENCY TO SQUARE WAVE CONVERTER (843).
- MOTHERBOARD (825):** Provides multiple input channels:
 - V1, V2, V3:** Voltage input signals.
 - I1, I2, I3, I4:** Current input signals, each with a corresponding voltage sense line (e.g., 866a, 868a).
 - CALIBRATION CONSTANTS EEPROM (839):** Stores calibration data.
 - DIO1, DIO3B:** Digital I/O signals.
- Interfacing and Output:**
 - SIGNAL CONDITIONING CIRCUITRY (823):** Processes signals from the MOTHERBOARD before they reach the digital converters.
 - VOLTAGE AND CURRENT INPUT SIGNALS (821):** The raw input signals from the MOTHERBOARD.
 - DIGITAL I/O TRANSCEIVERS (849):** Manage digital communication between the MOTHERBOARD and the CPU BOARD.
 - DIGITAL INPUT/OUTPUT BUS (845):** Connects the transceivers to the CPU BOARD.
 - DISPLAY (851):** Provides visual feedback, connected to the CPU BOARD.
 - COMMUNICATIONS BOARD (848):** Includes:
 - OPTICAL ISOLATION (852):** Protects the communication interface.
 - SERIAL COMMUNICATION TRANSCEIVERS (853):** Handle RS-232 and RS-485 signals.
 - ASYNCHRONOUS SERIAL COMMUNICATION BUS (847):** Connects to the CPU BOARD.
 - SYNCHRONOUS SERIAL COMMUNICATIONS BUS (838):** Connects the CPU BOARD to the COMMUNICATIONS BOARD.

DATA ACQUISITION
MODULE
OPERATION (CLIENT
PORTION)

FIG. 11A

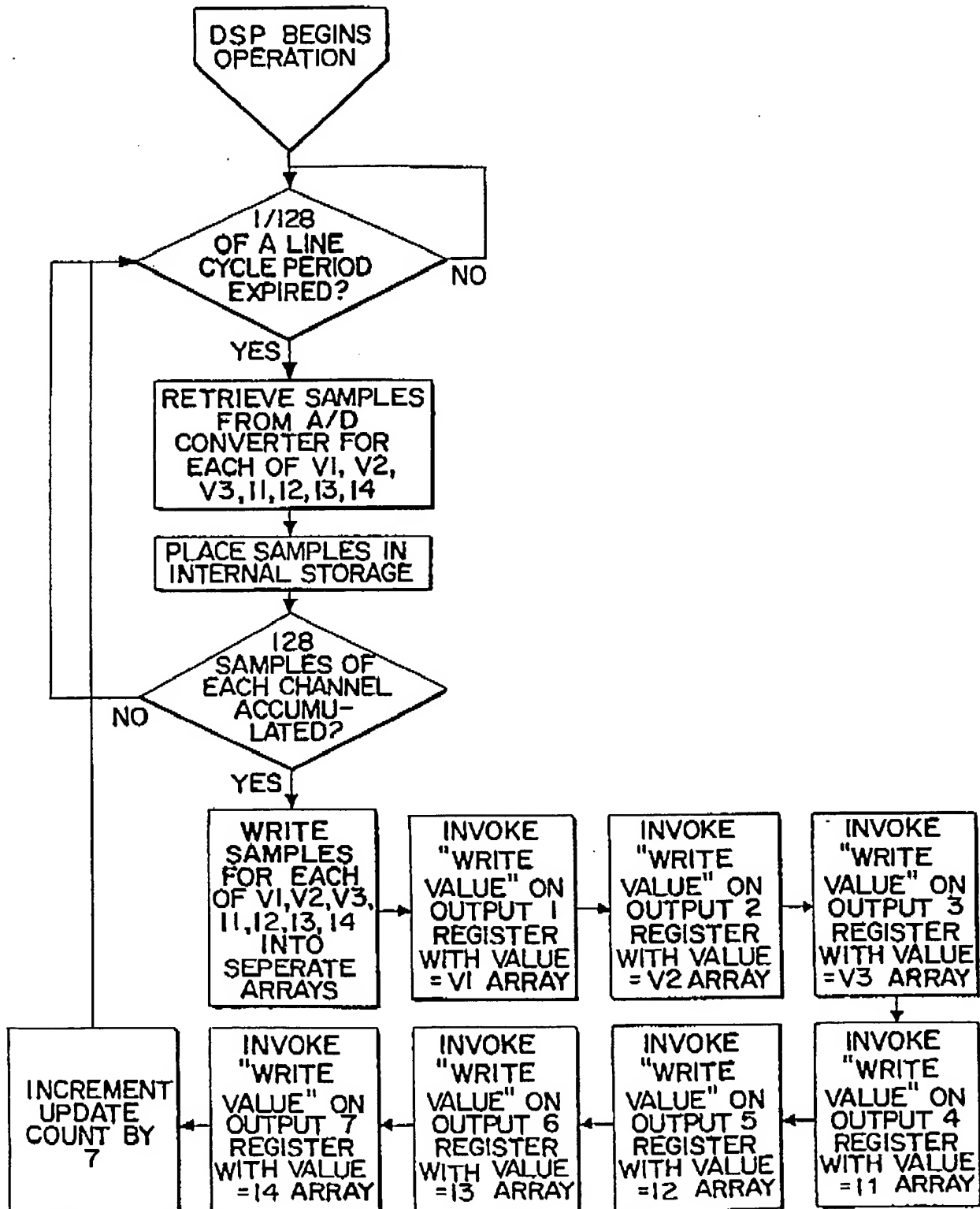
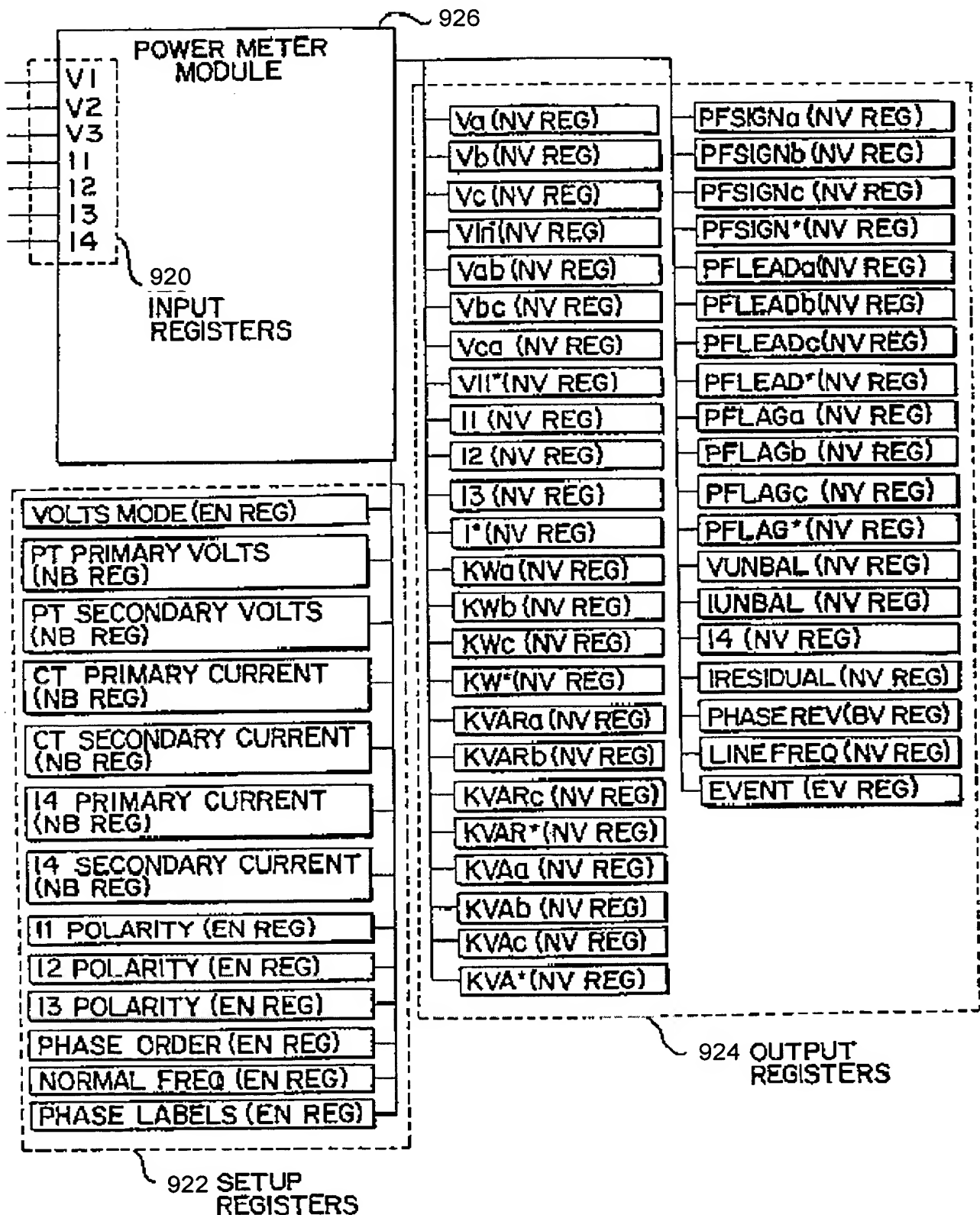
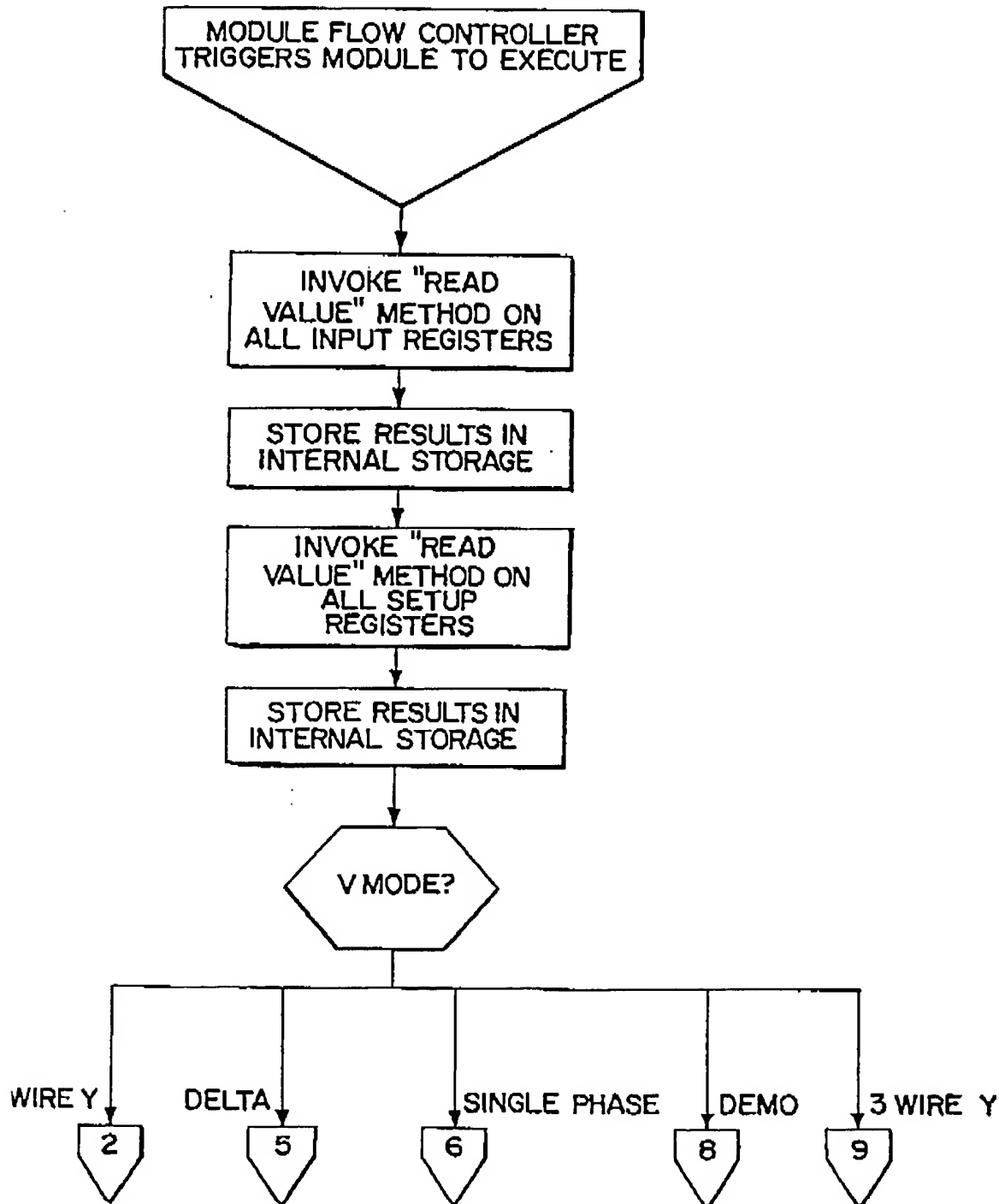


FIG. 12



POWER METER
MODULE
OPERATION
(CLIENT PORTION)

FIG. 12A



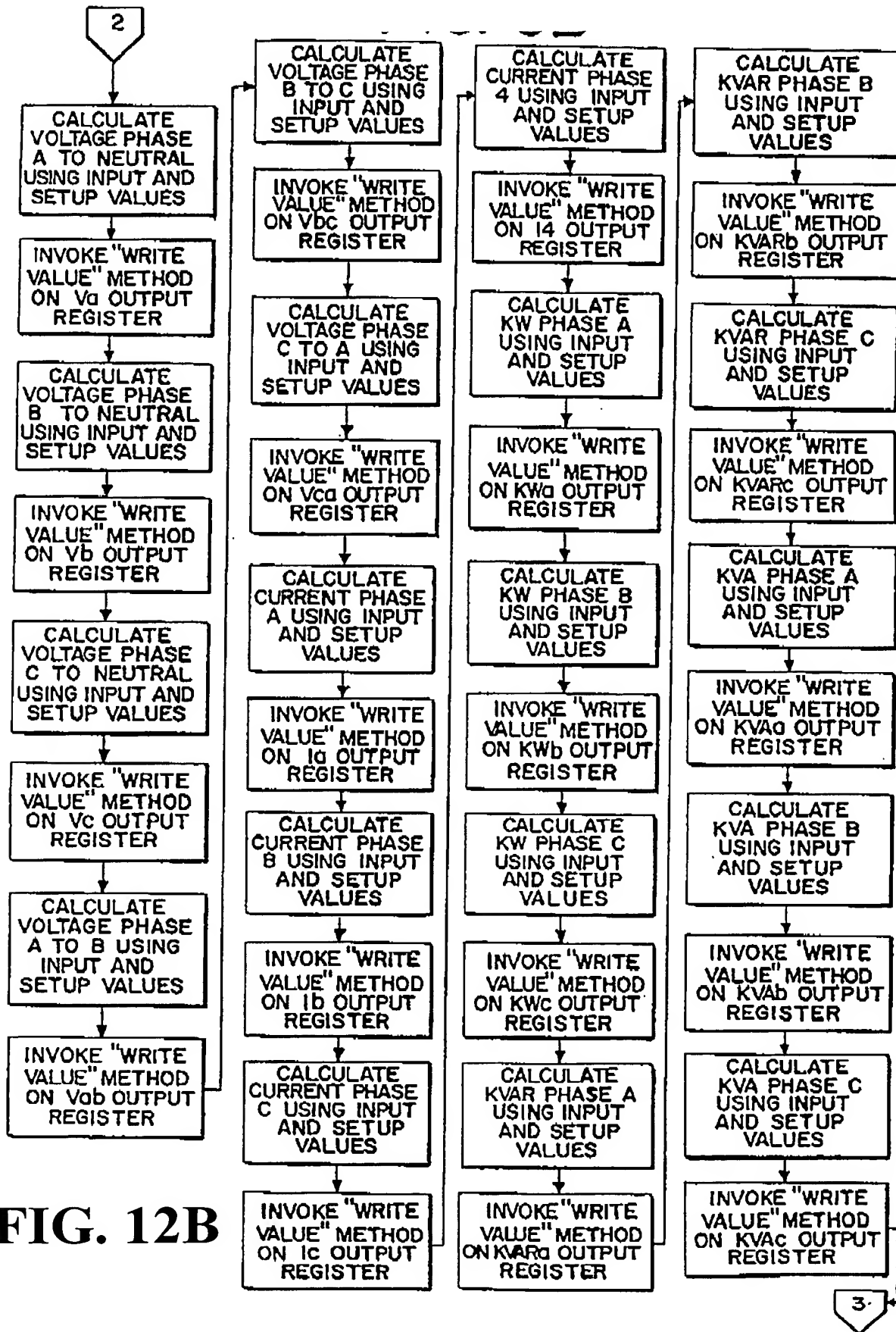


FIG. 12C

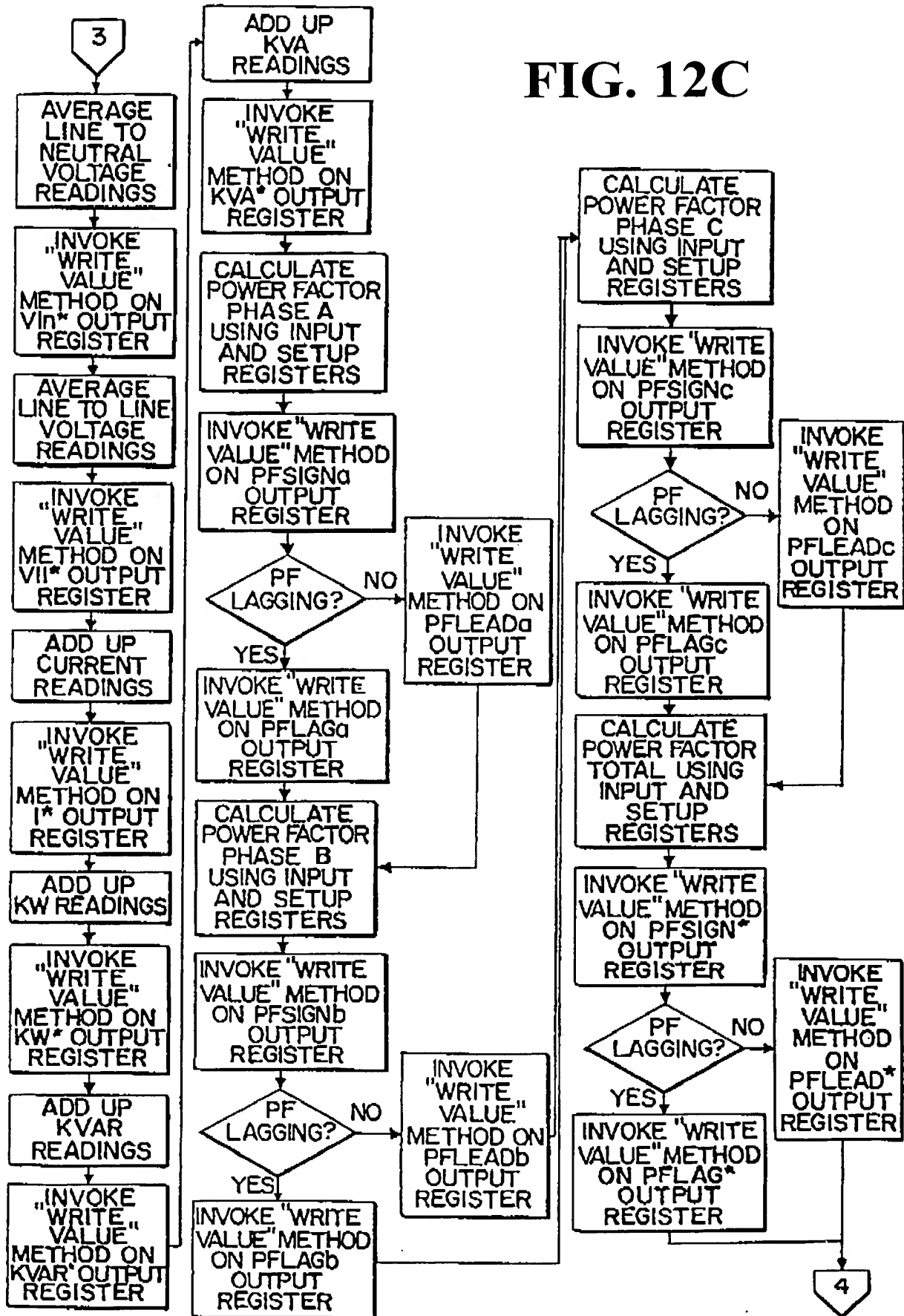


FIG. 12D

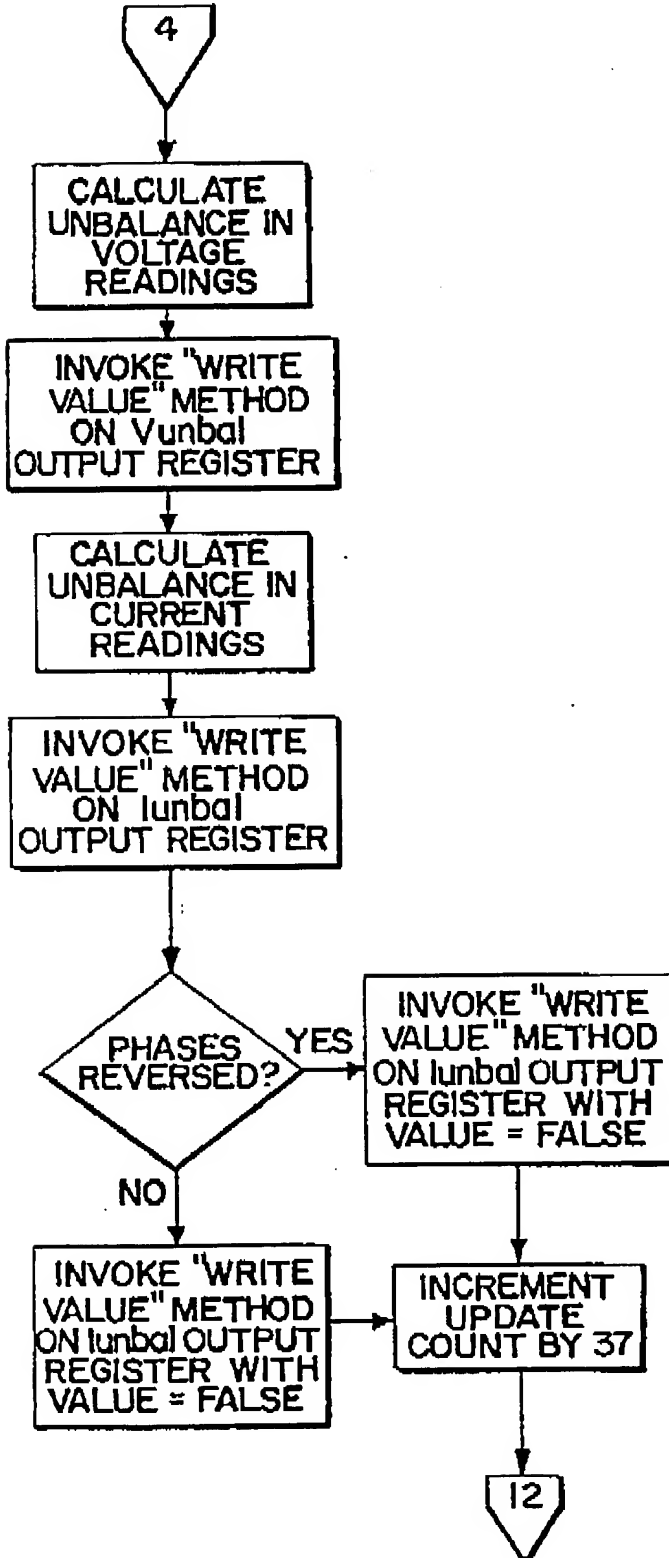


FIG. 12H

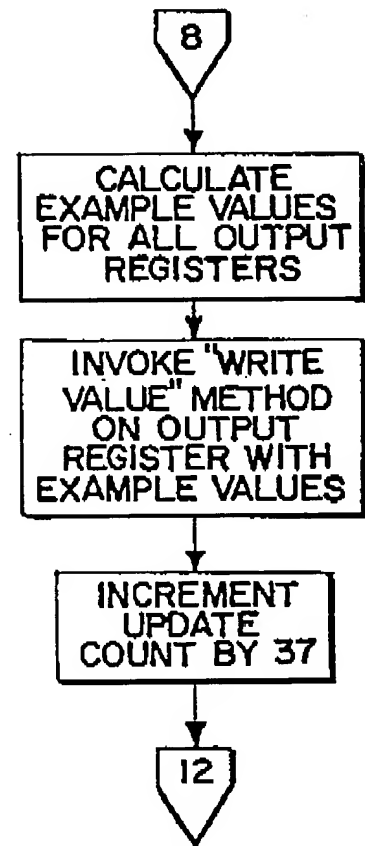


FIG. 12E

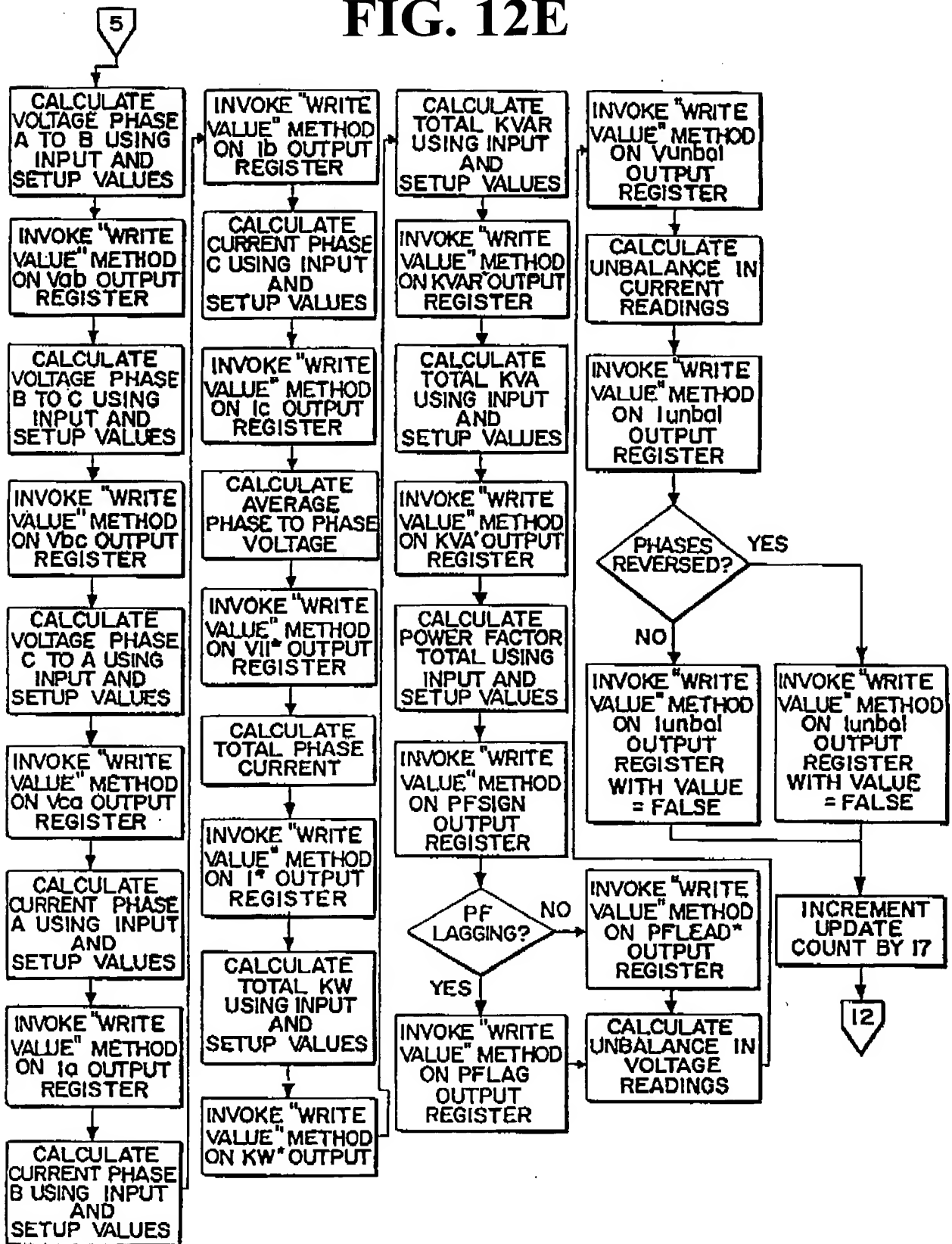


FIG. 12F

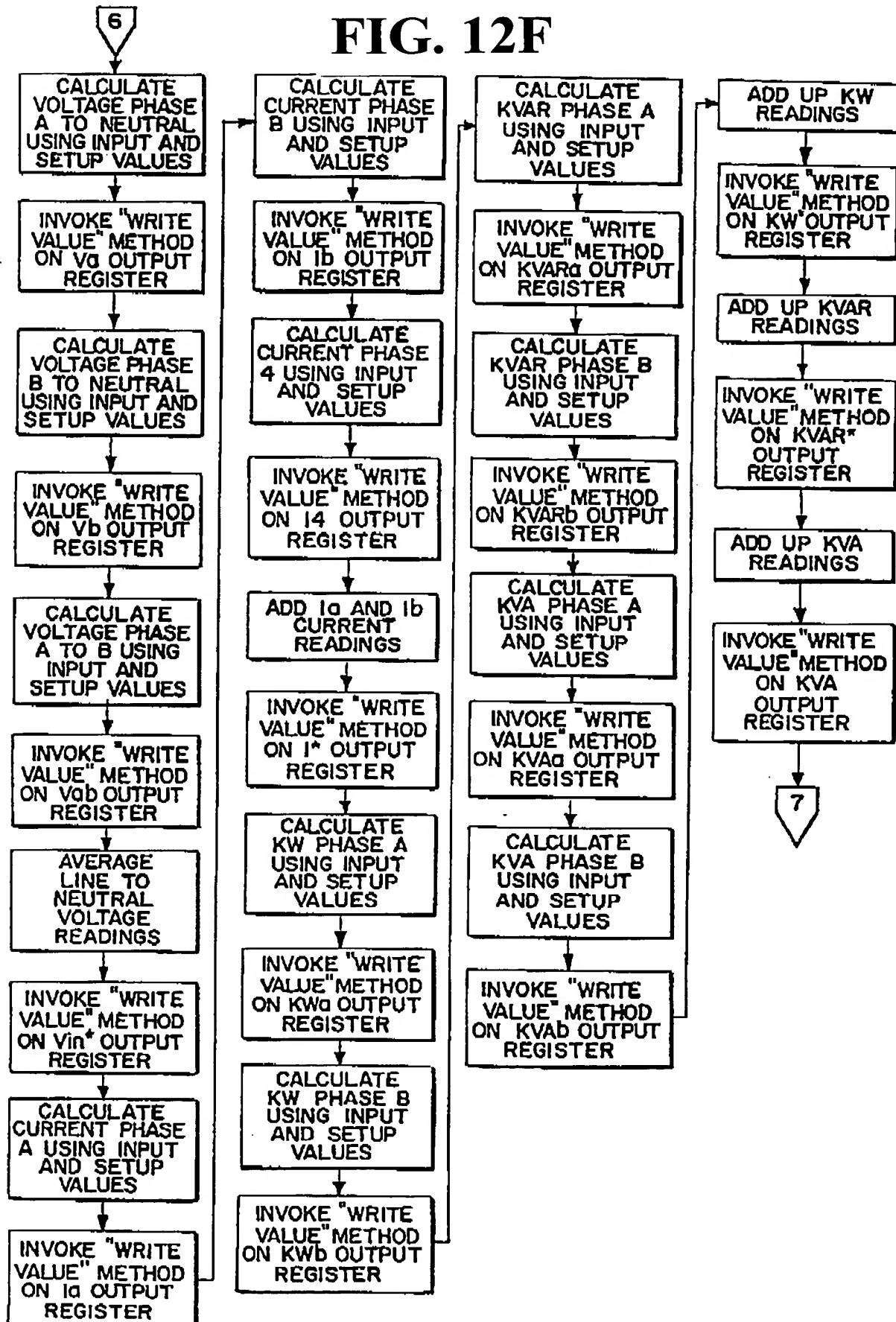
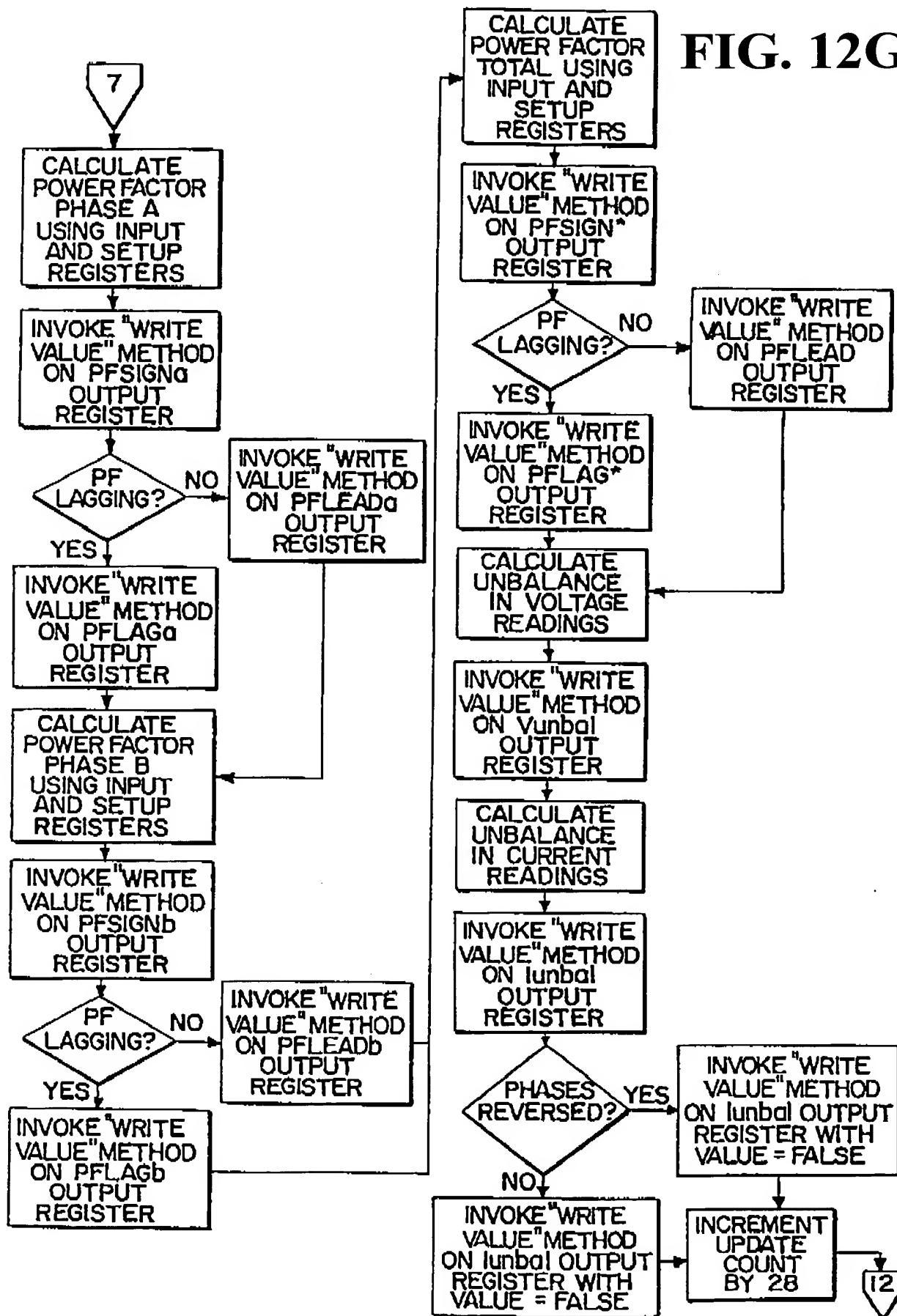


FIG. 12G



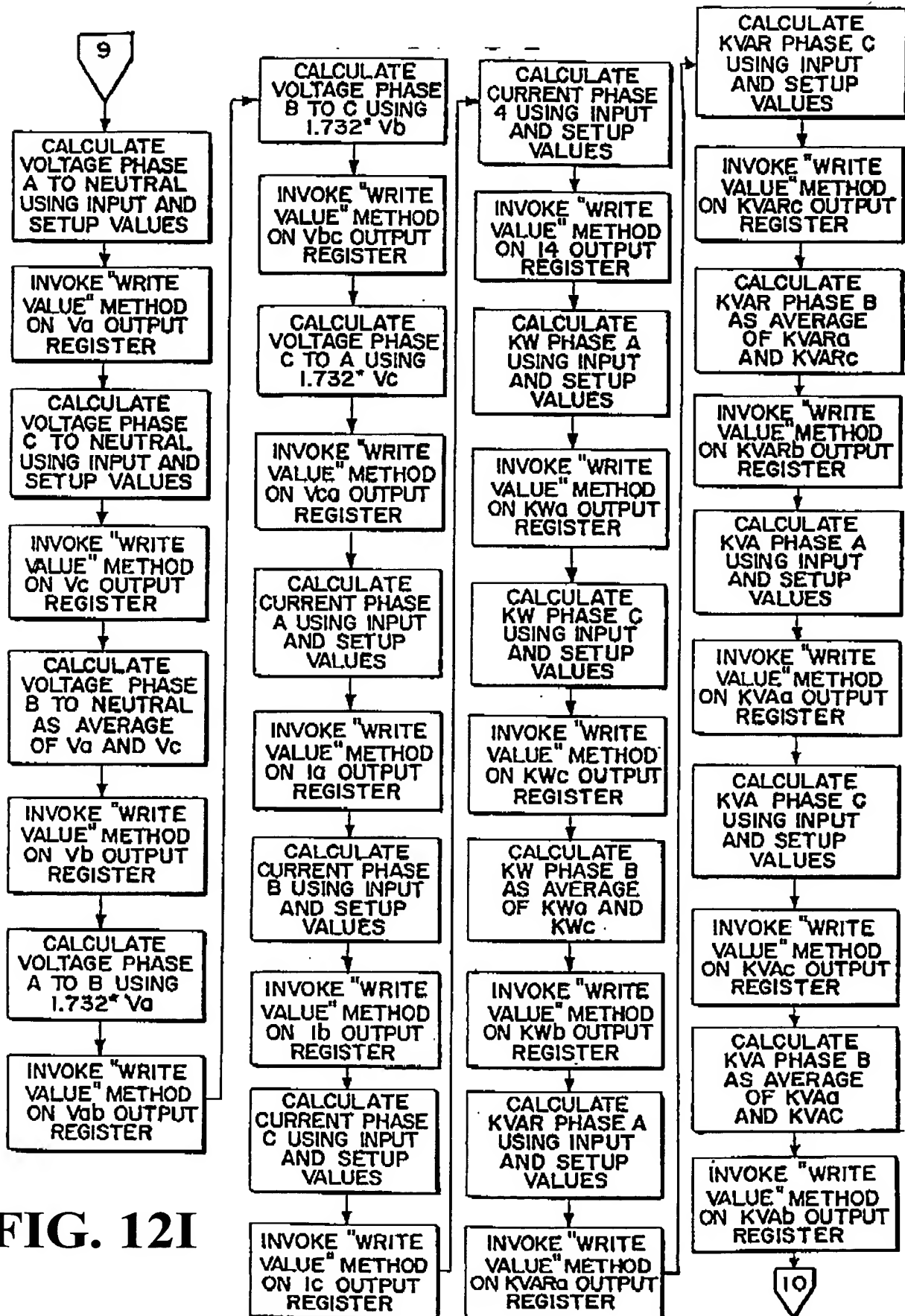


FIG. 12I

FIG. 12J

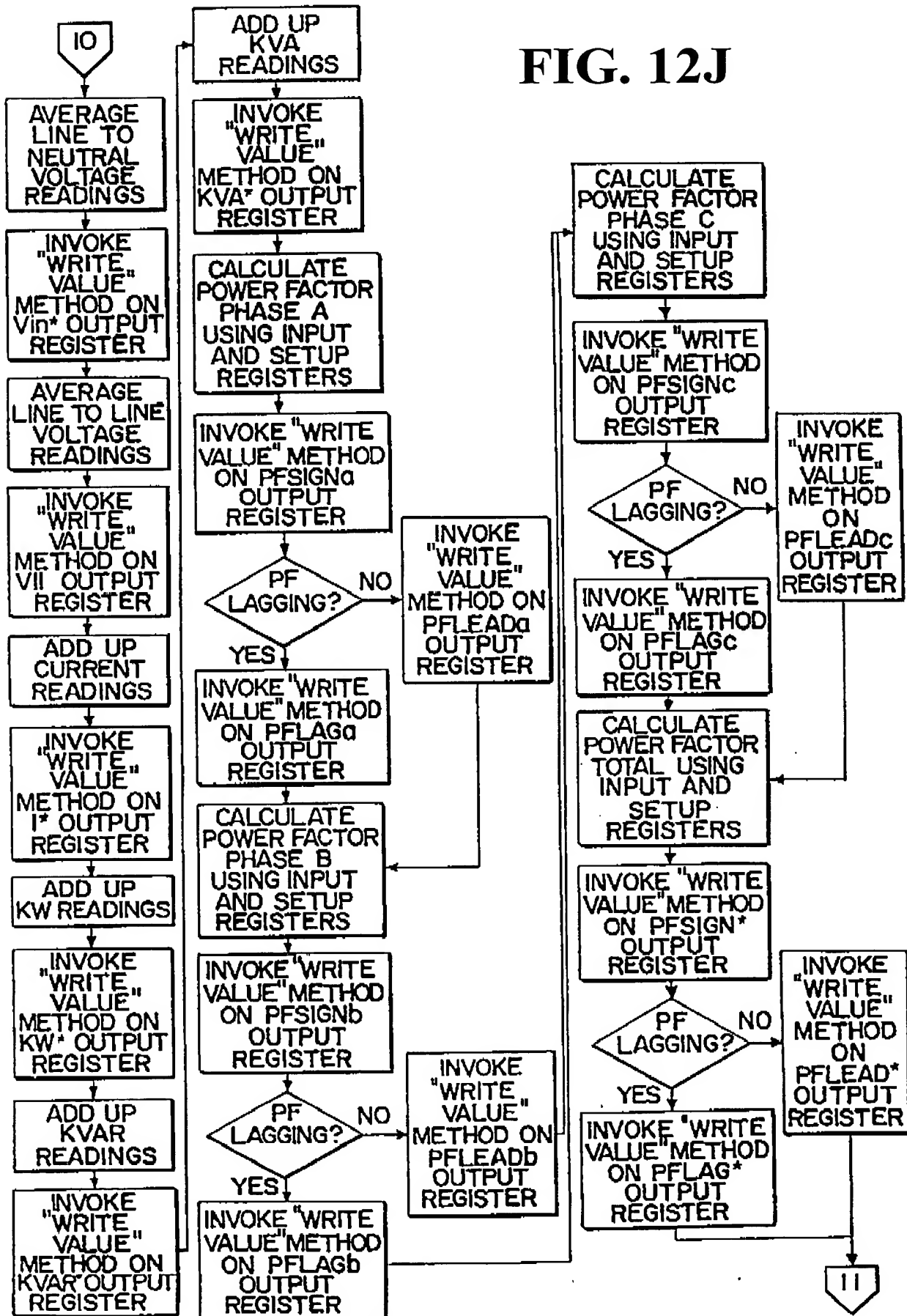


FIG. 12K

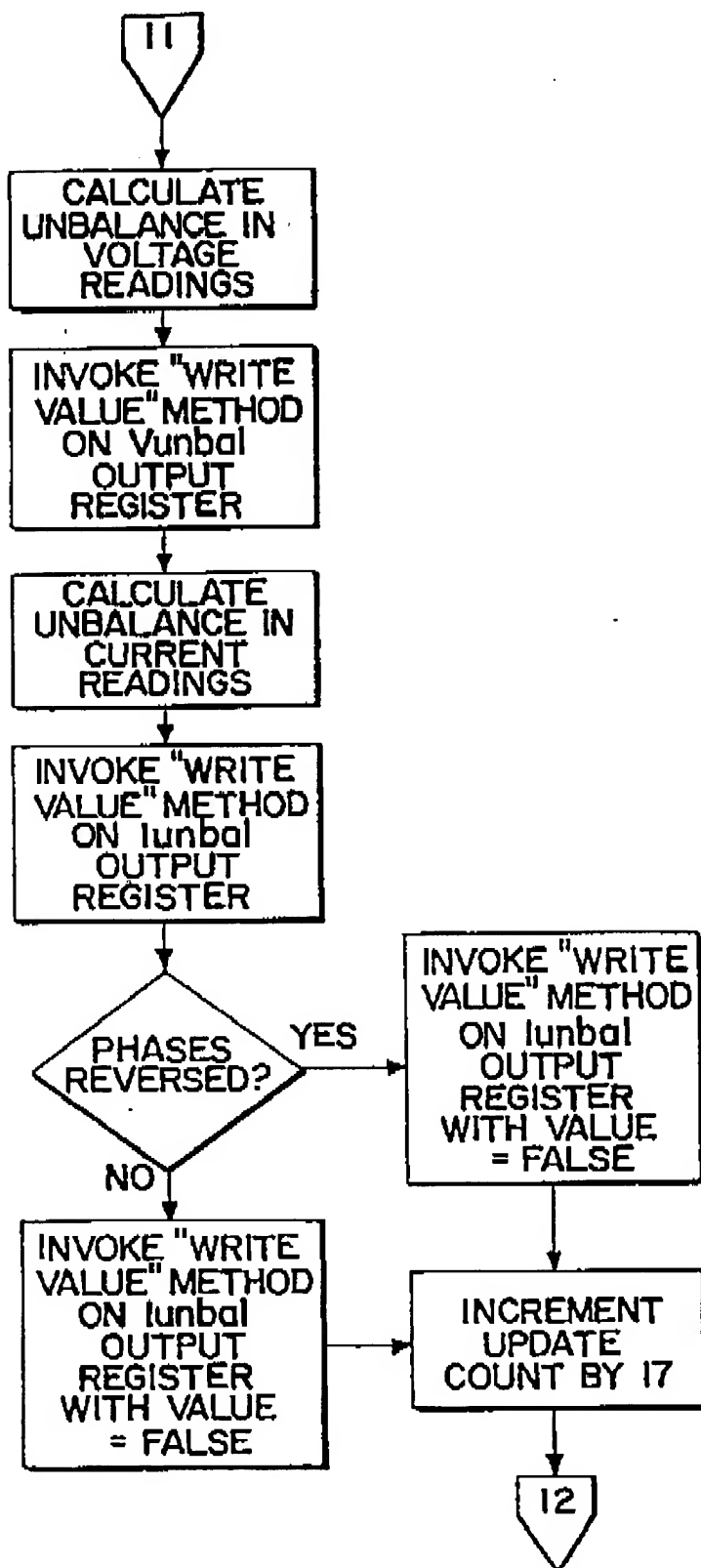


FIG. 12L

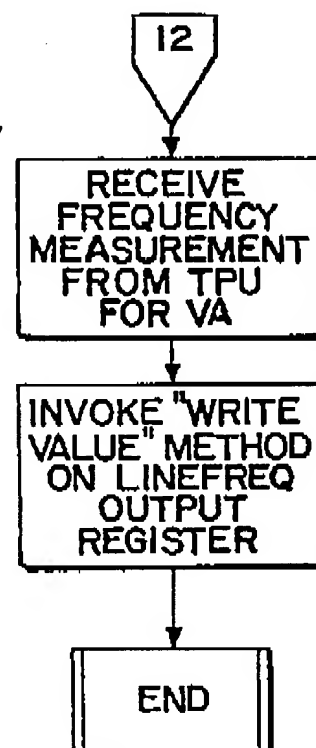


FIG. 13

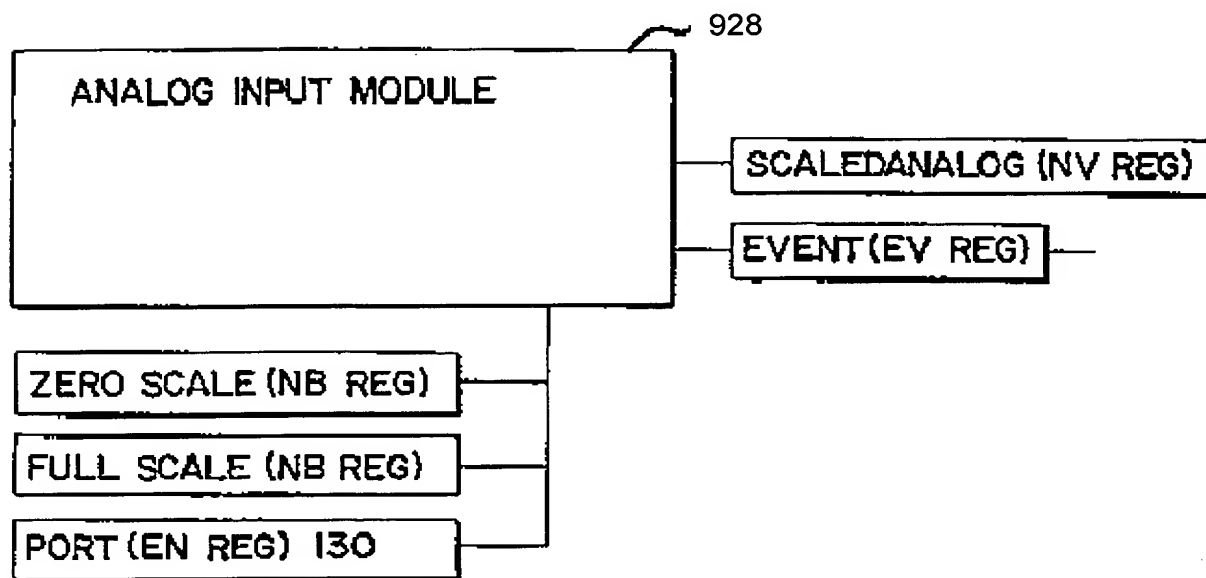


FIG. 14

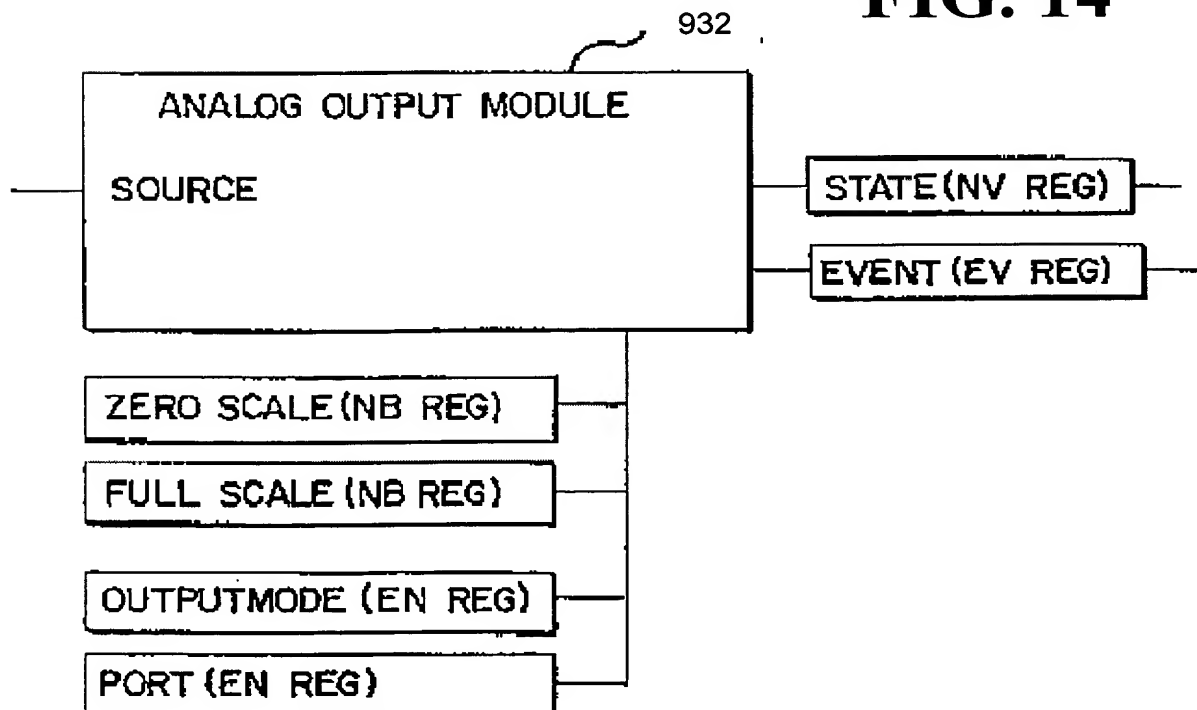


FIG. 13A

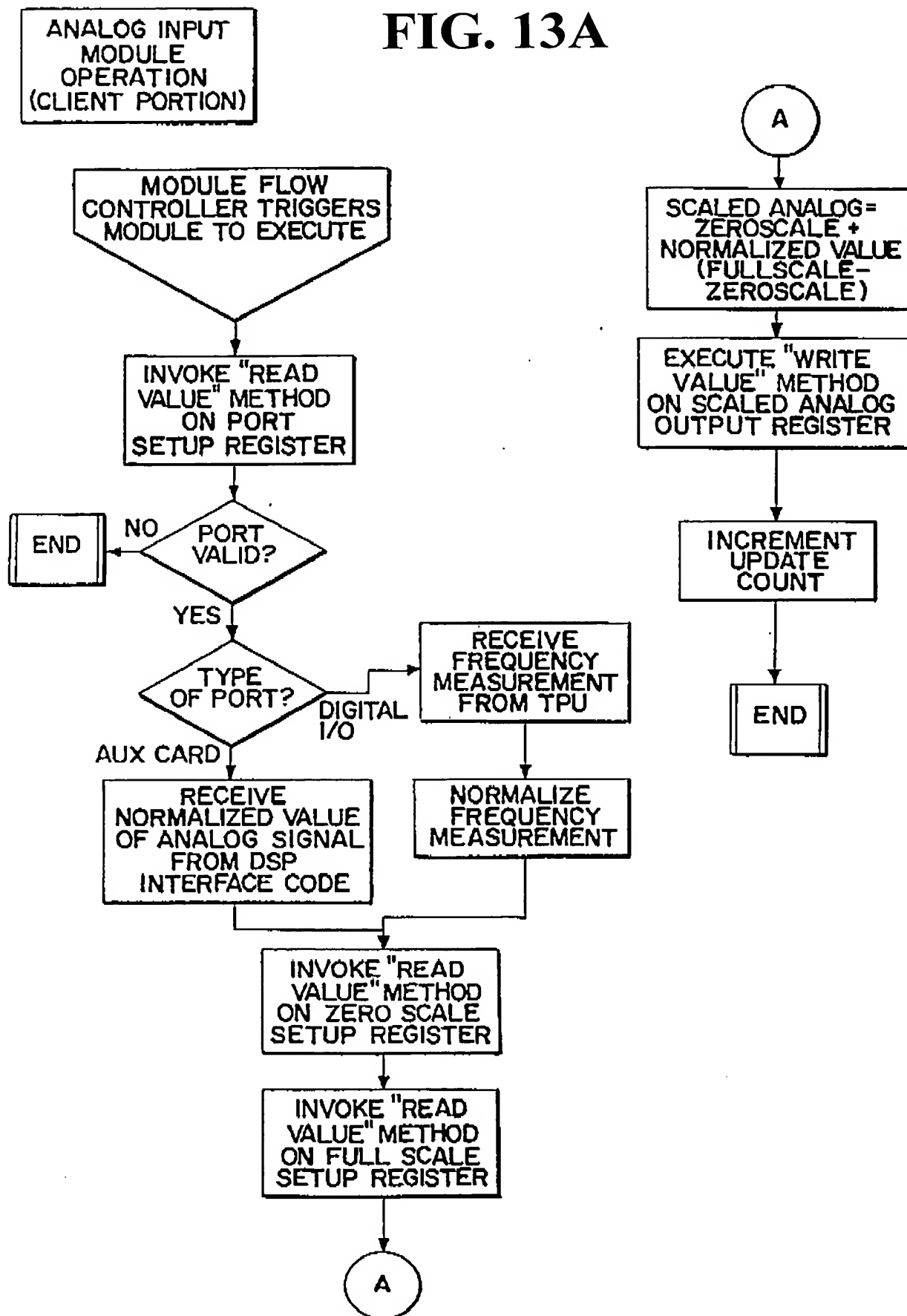


FIG. 14A

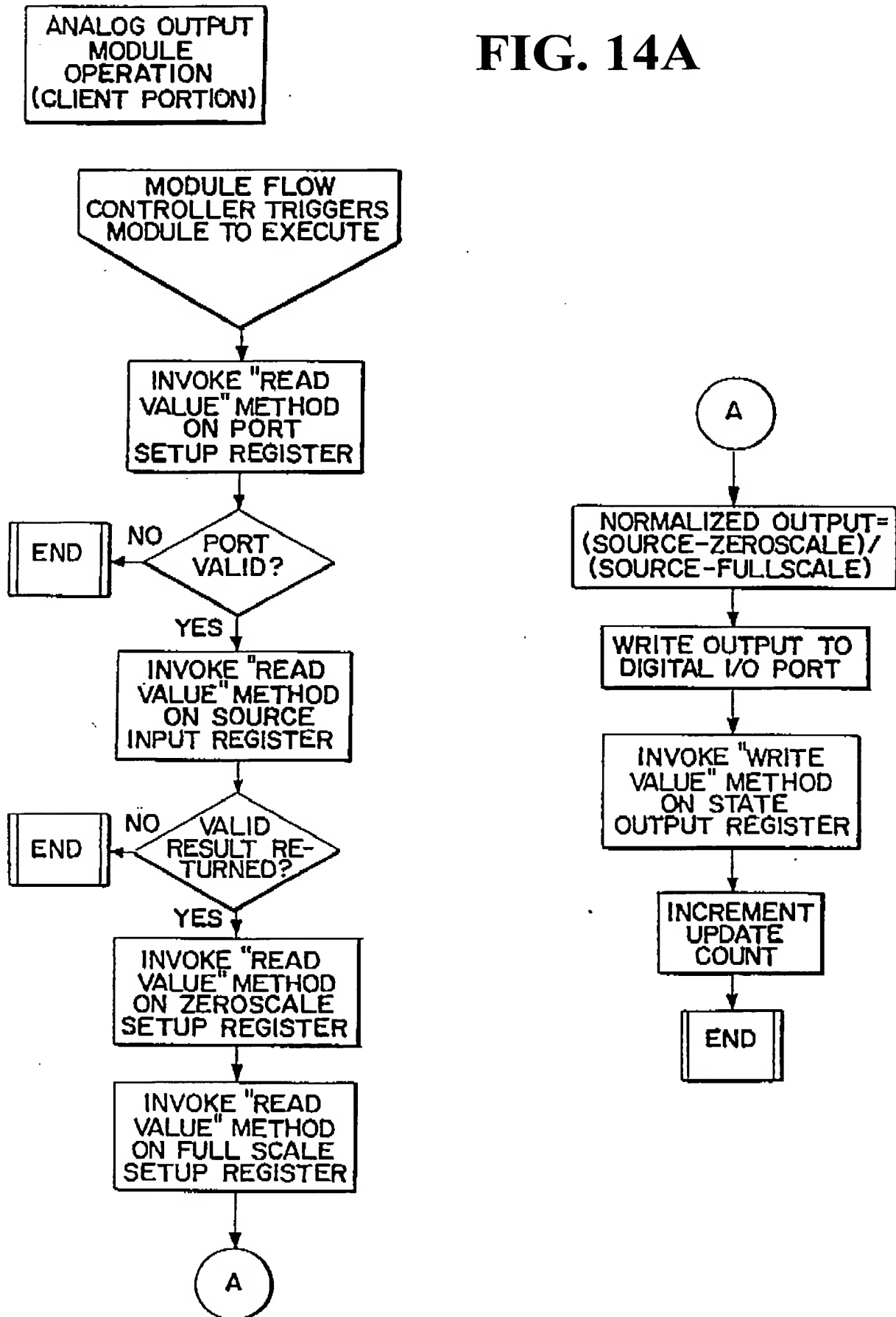


FIG. 15

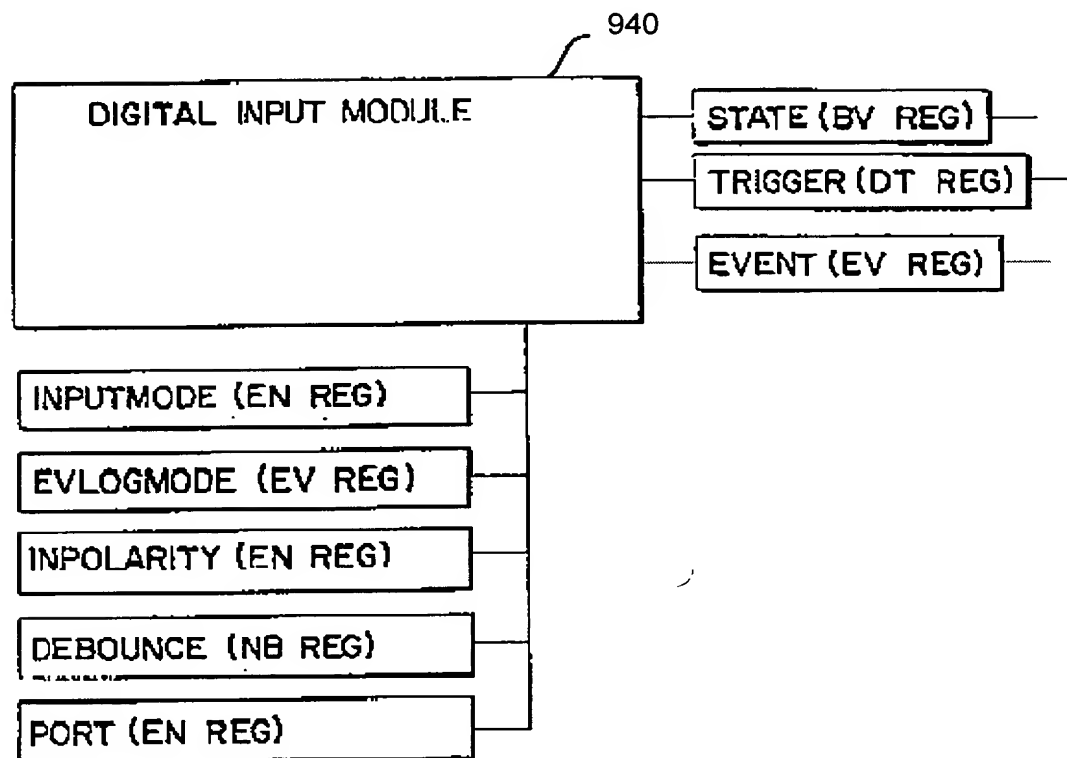


FIG. 16

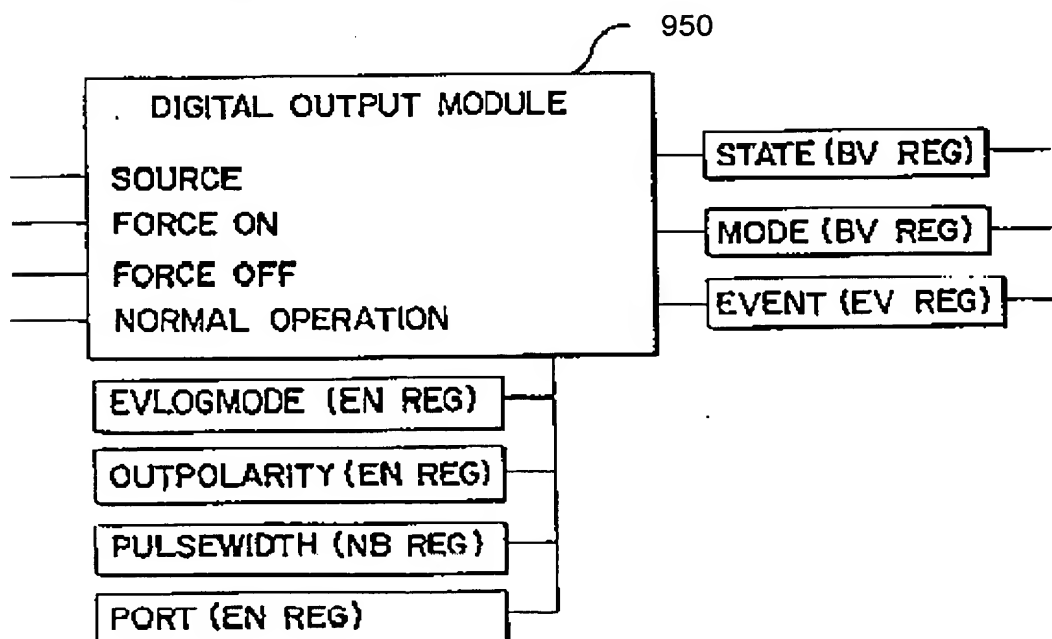


FIG. 15A

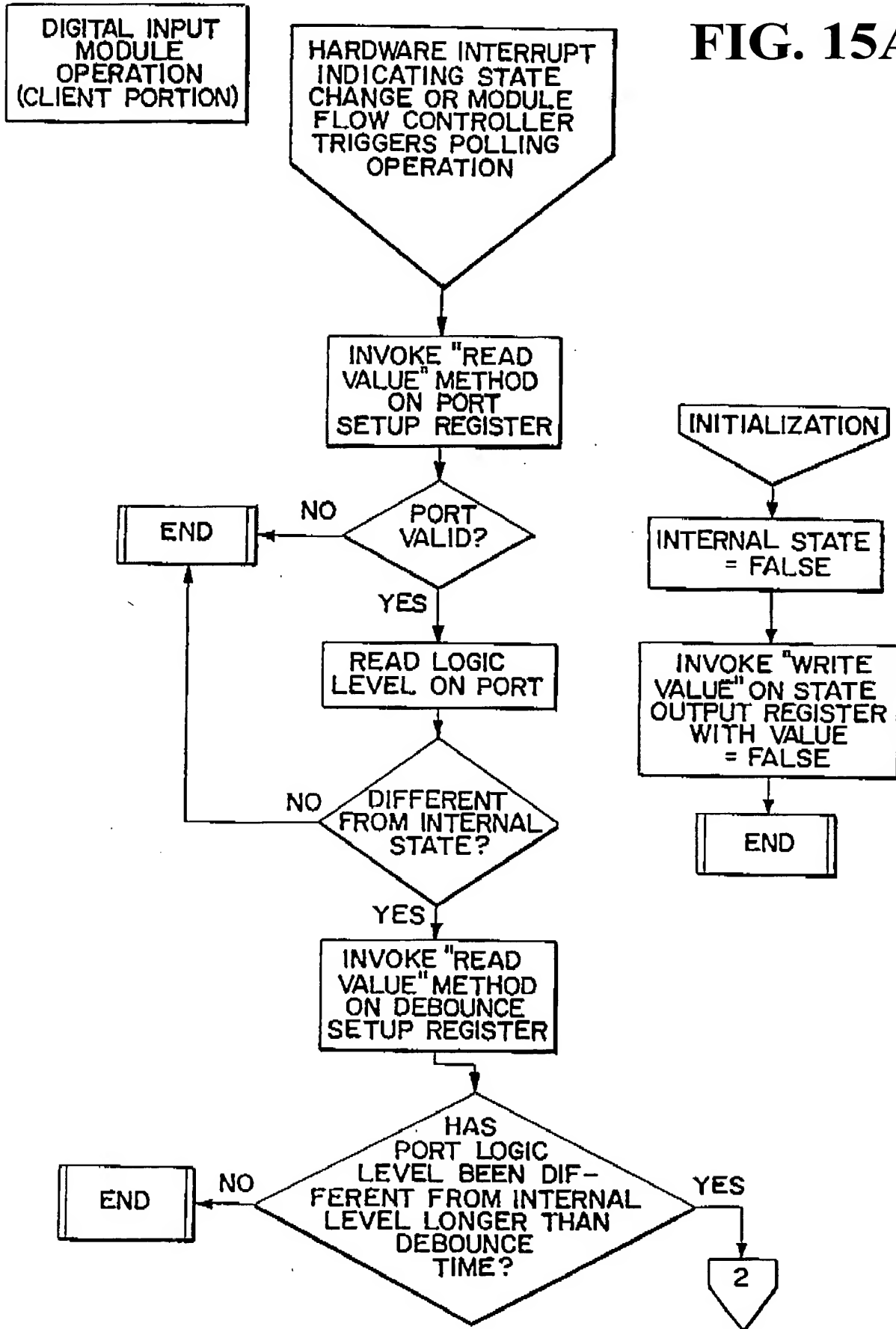
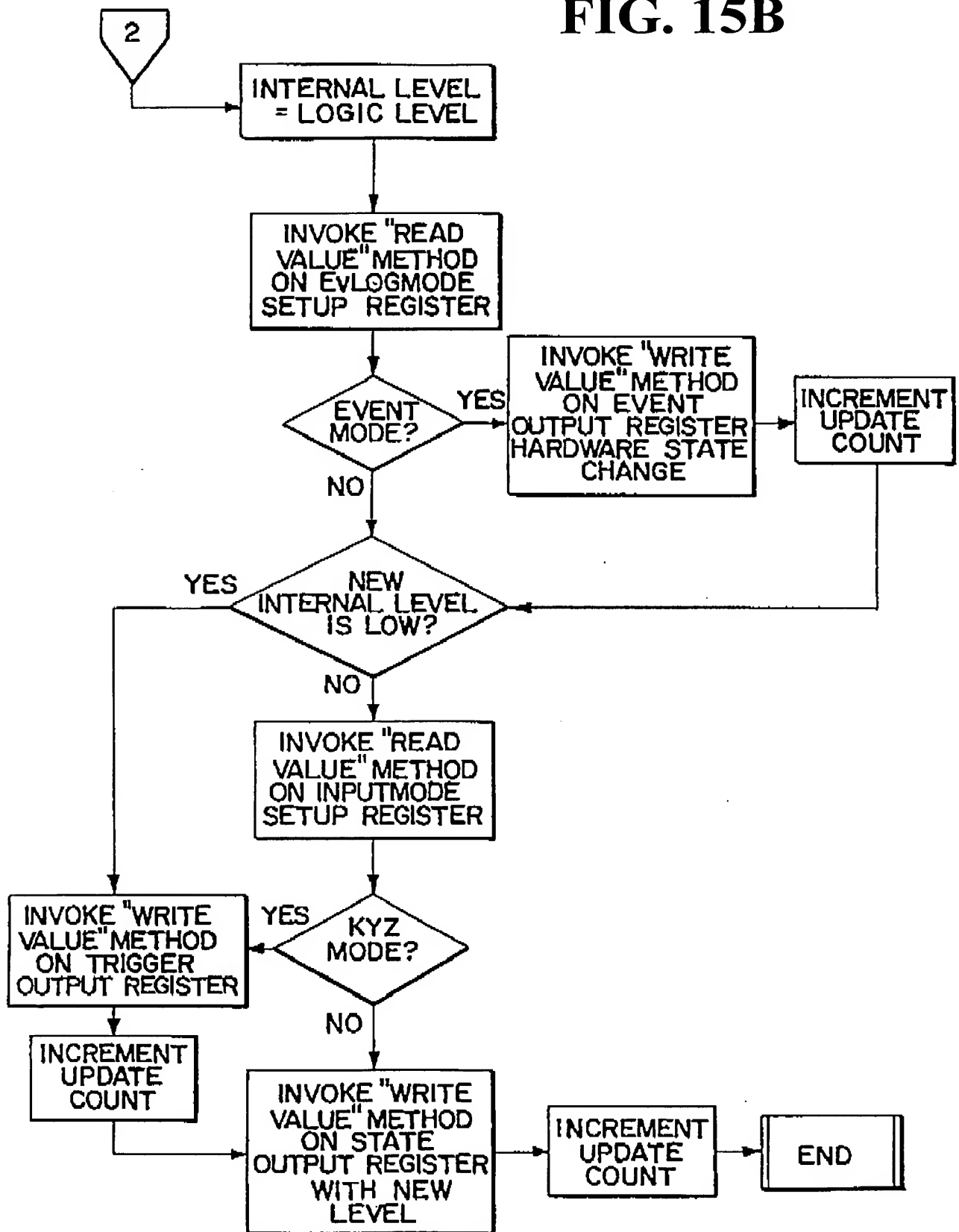


FIG. 15B



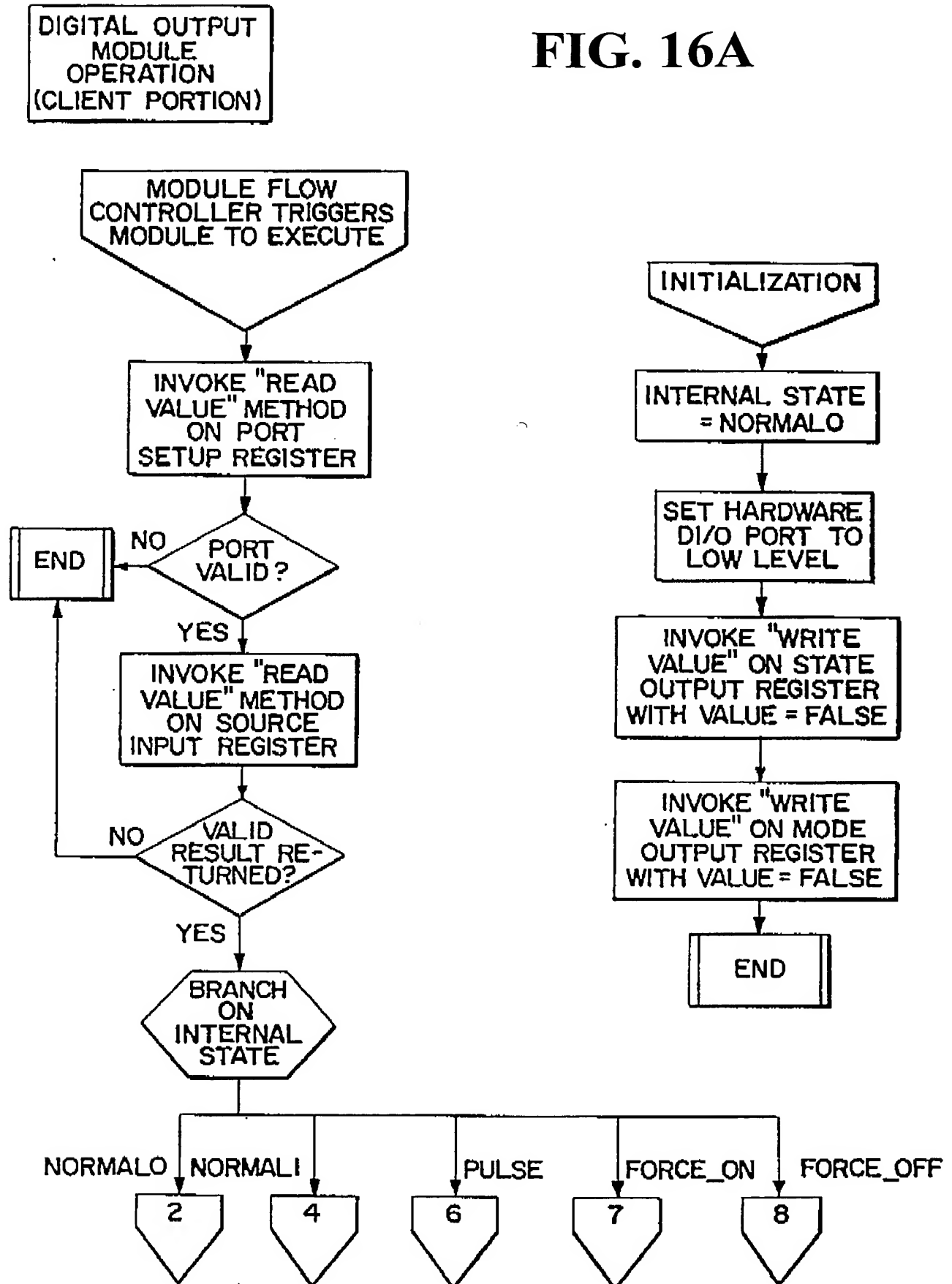


FIG. 16B

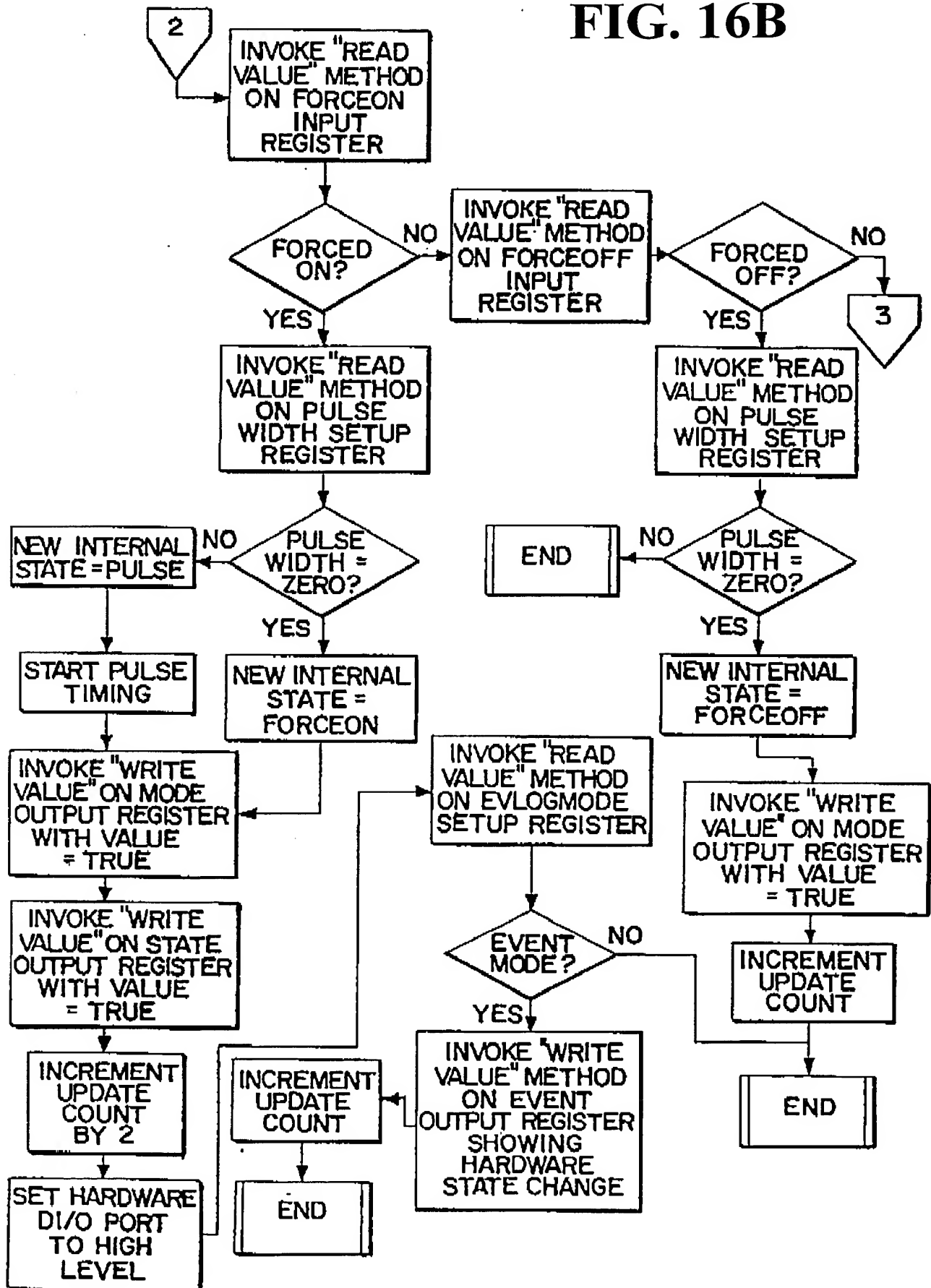


FIG. 16C

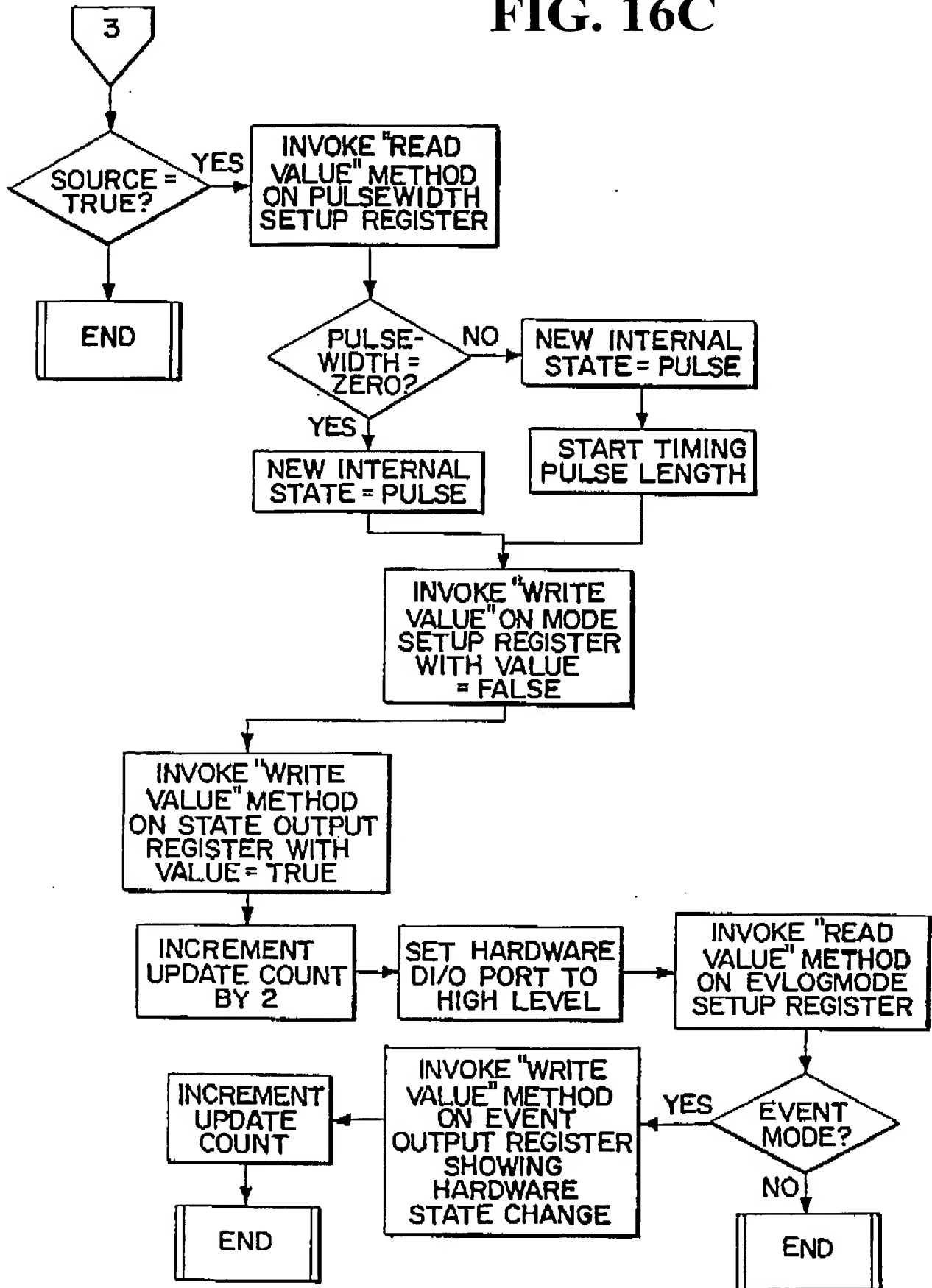


FIG. 16D

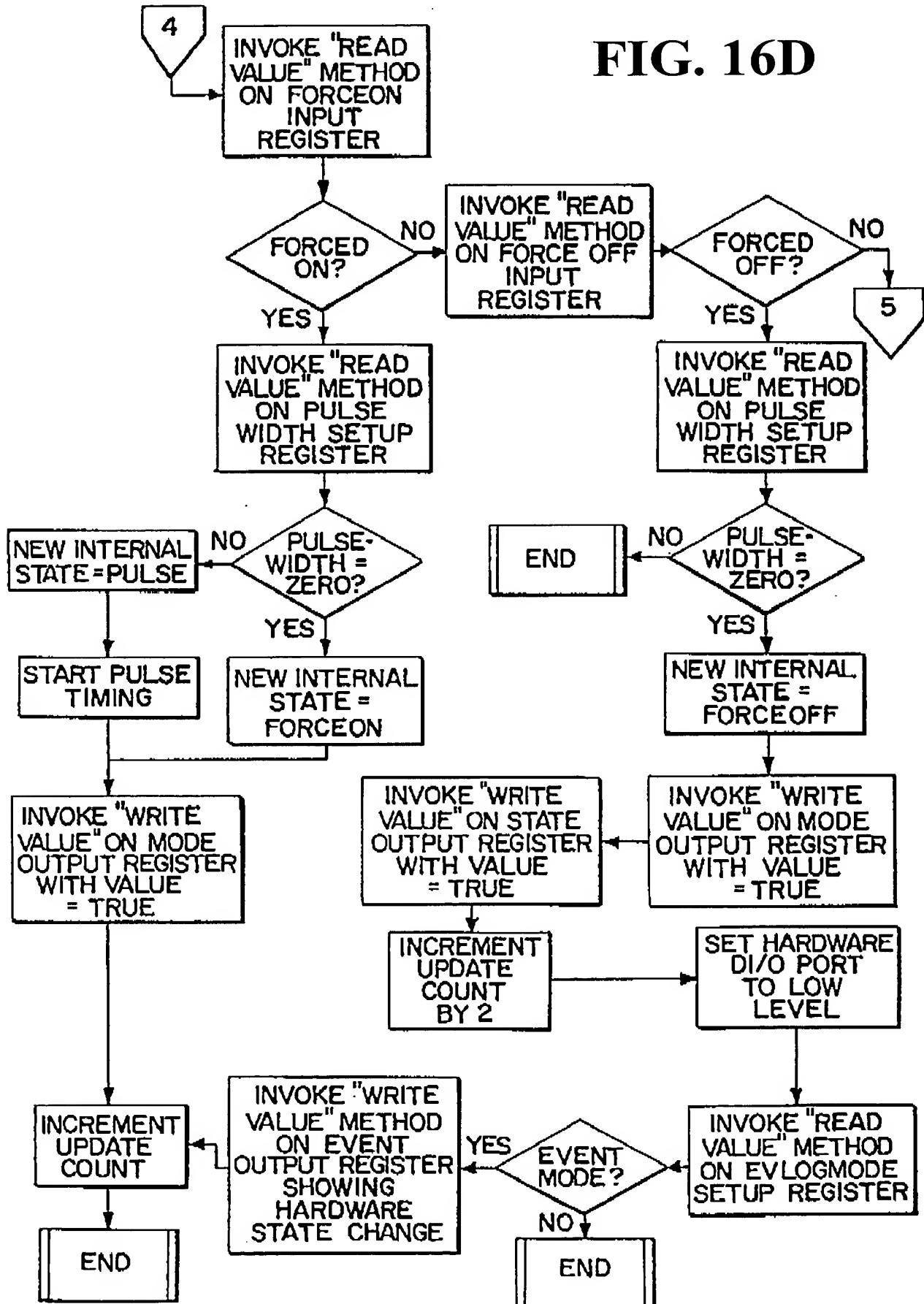


FIG. 16E

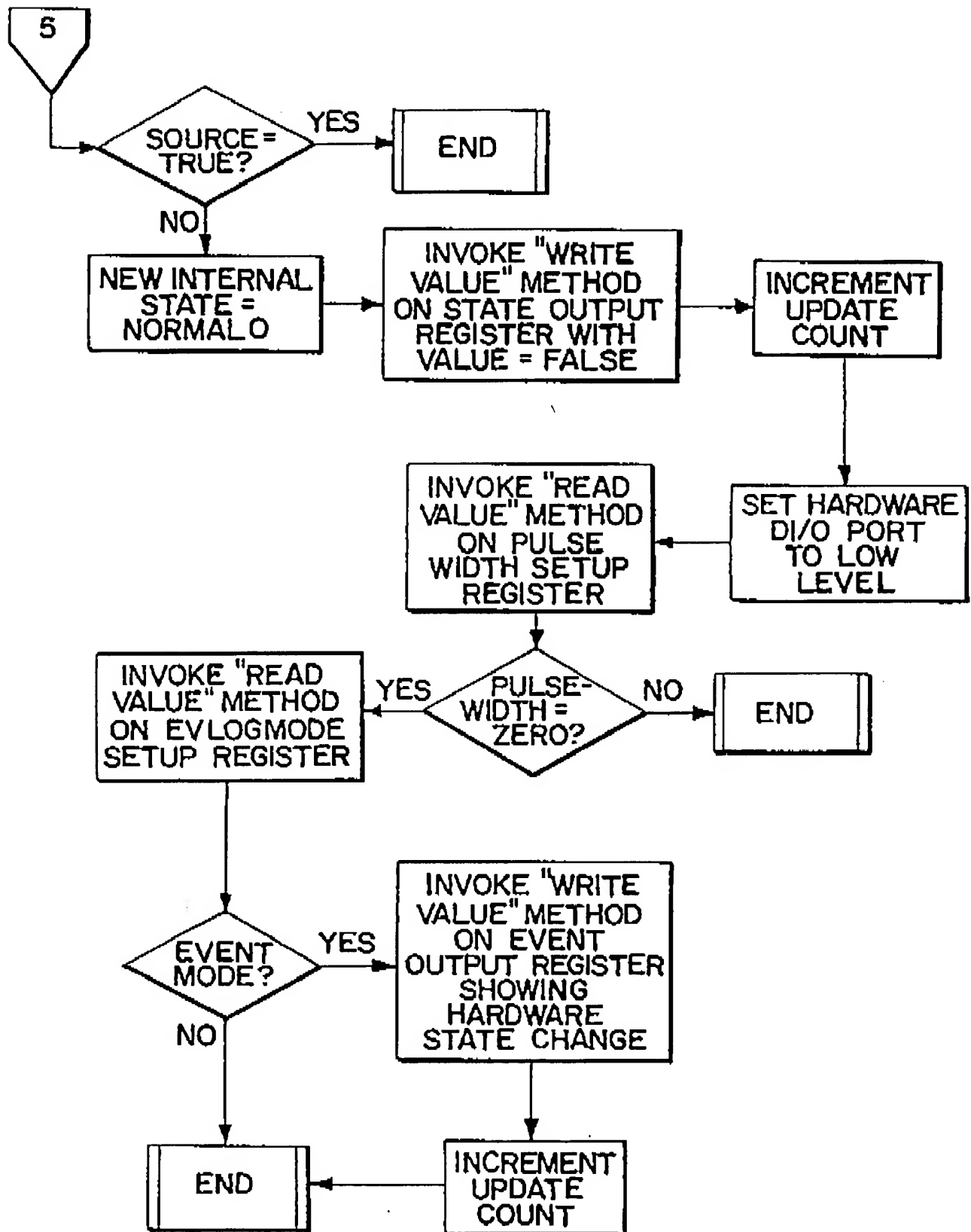


FIG. 16F

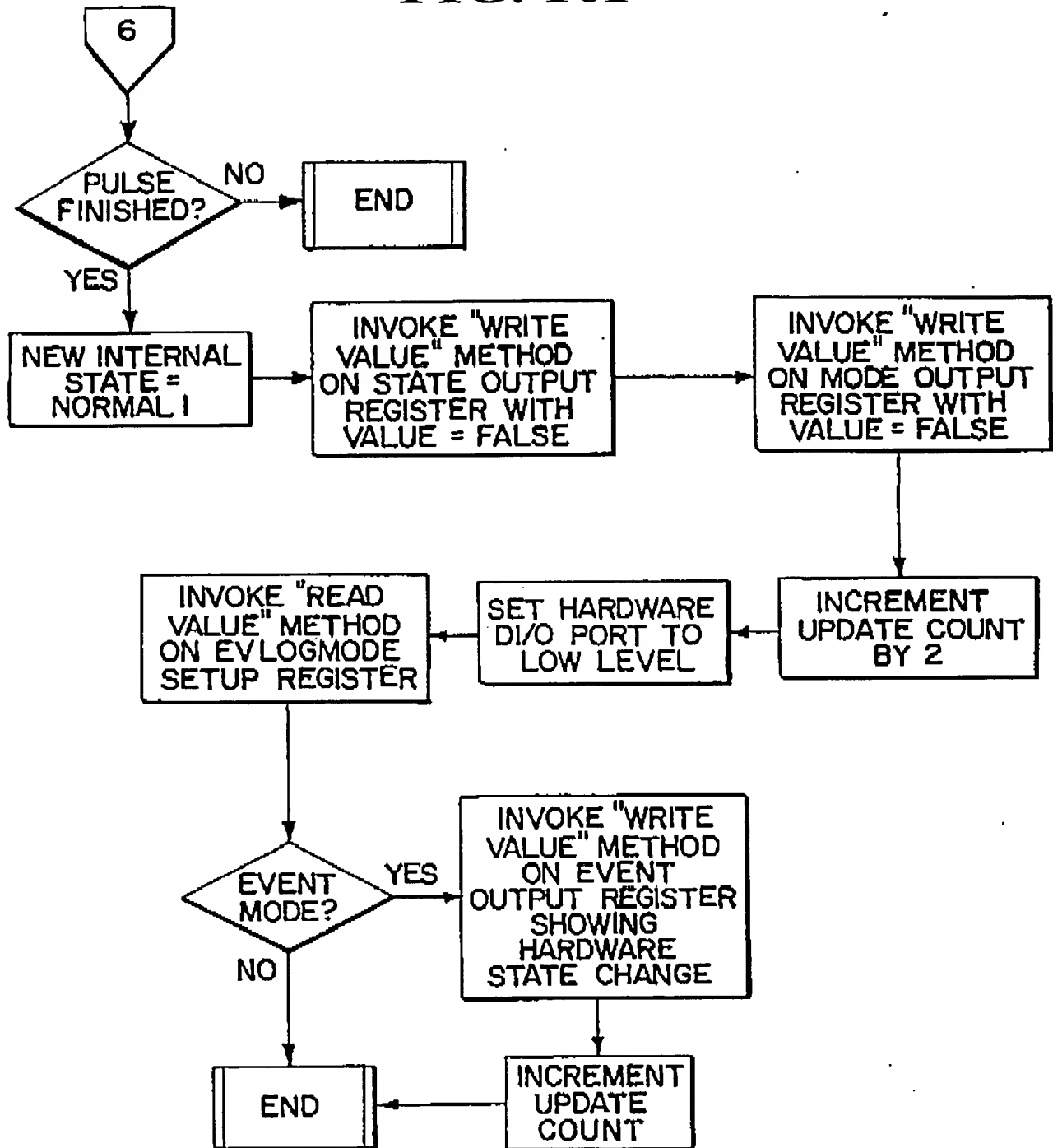


FIG. 16G

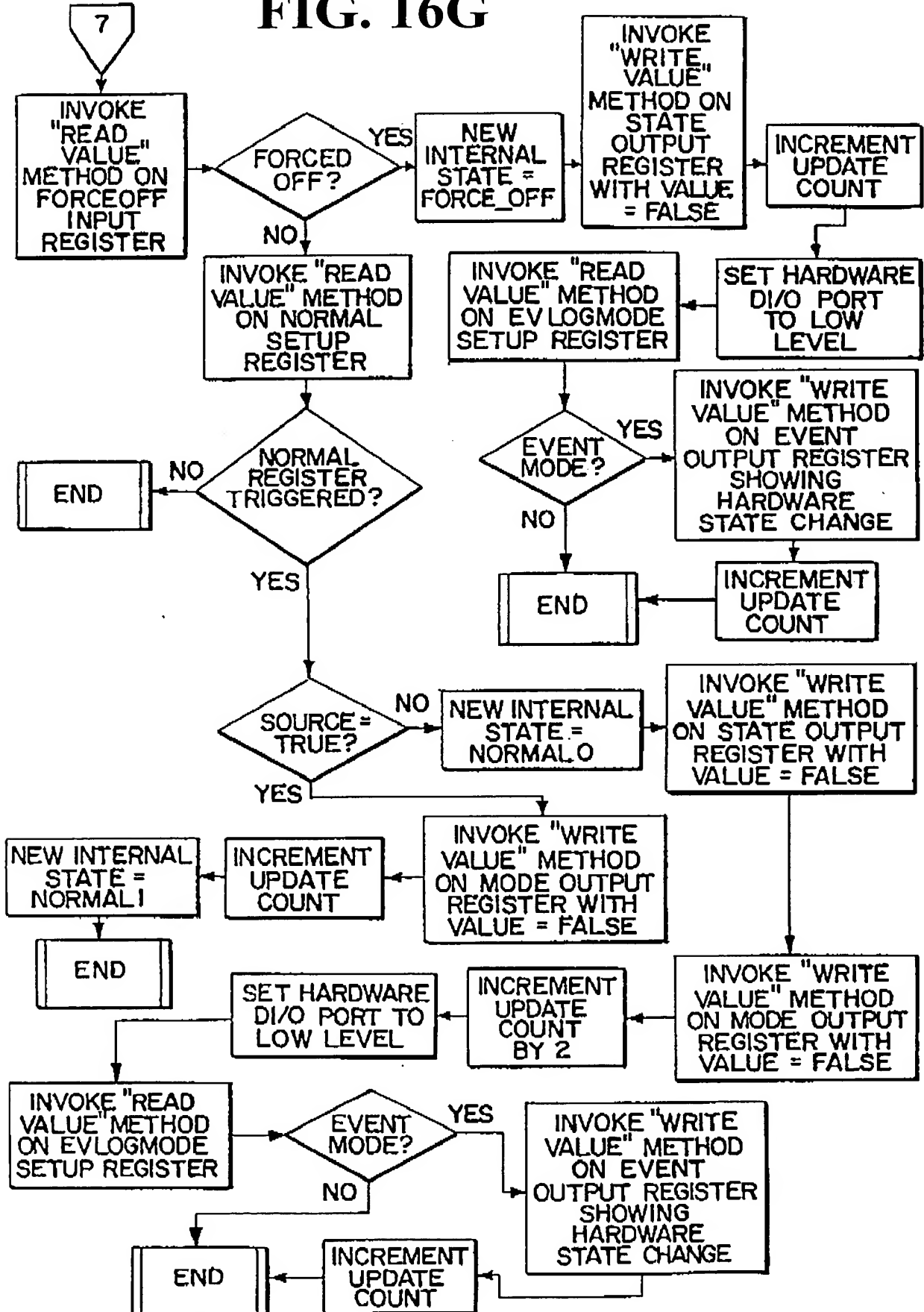


FIG. 16H

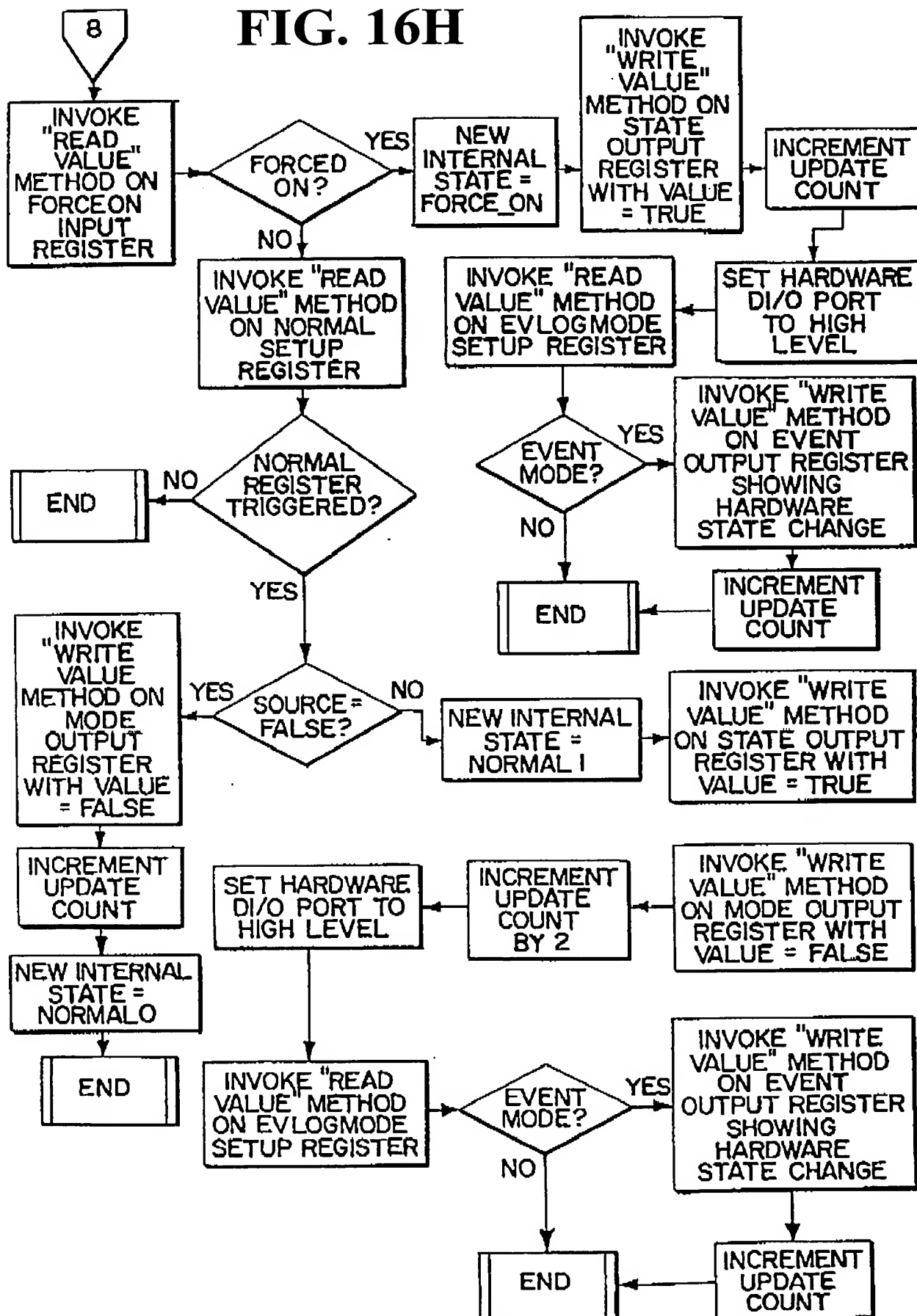


FIG. 17

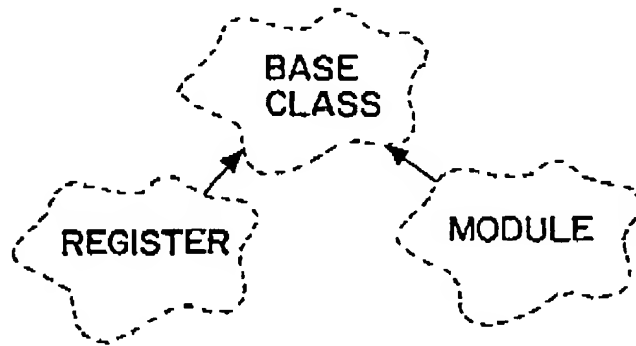


FIG. 17A

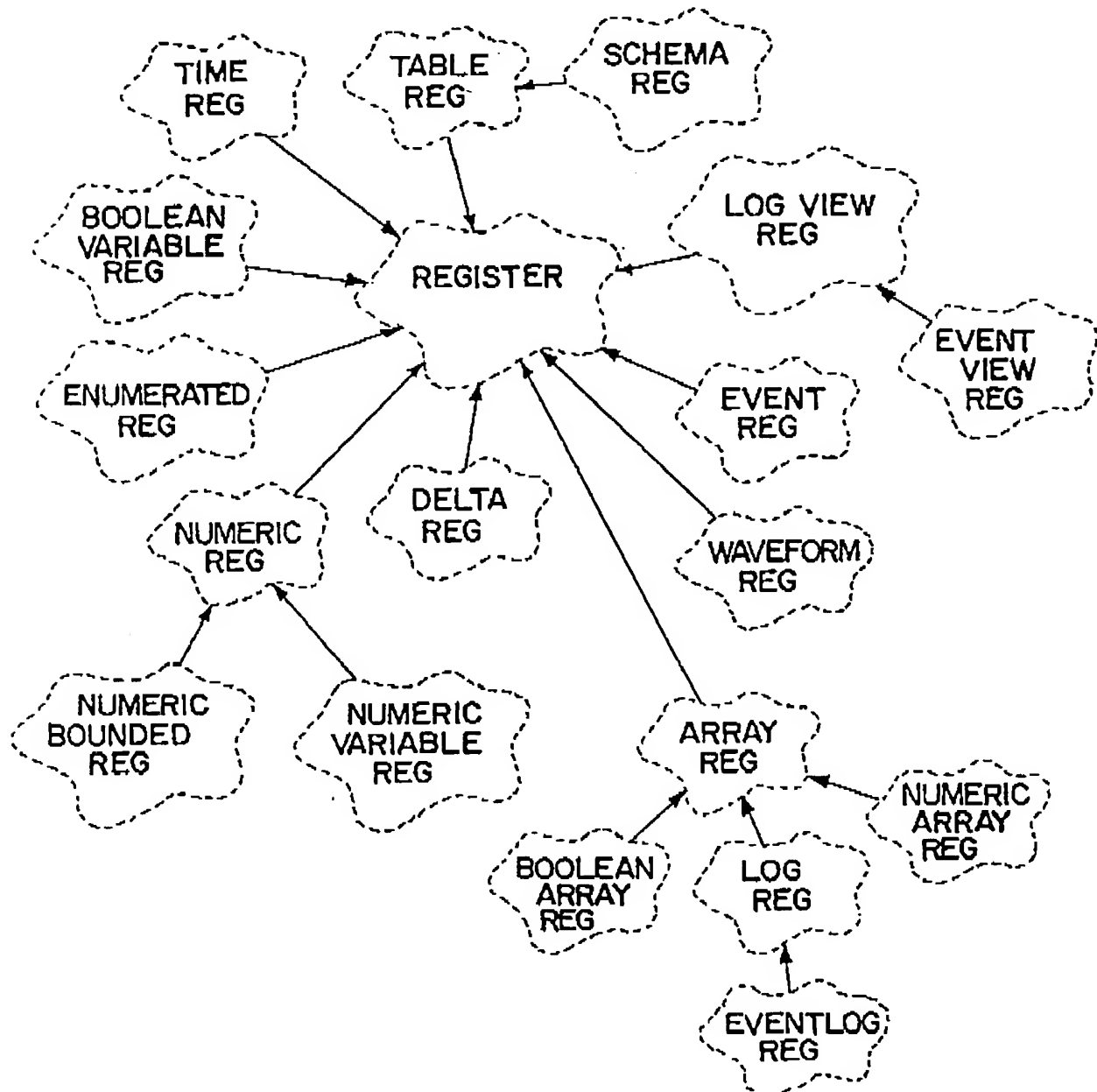


FIG. 17B

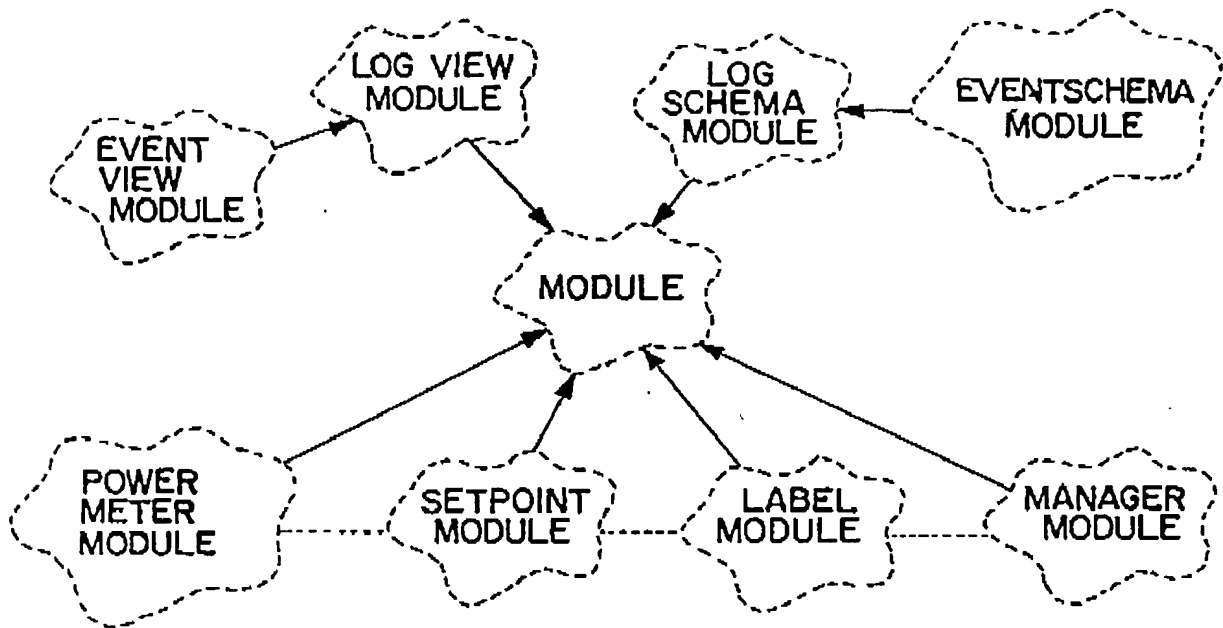


FIG. 17C

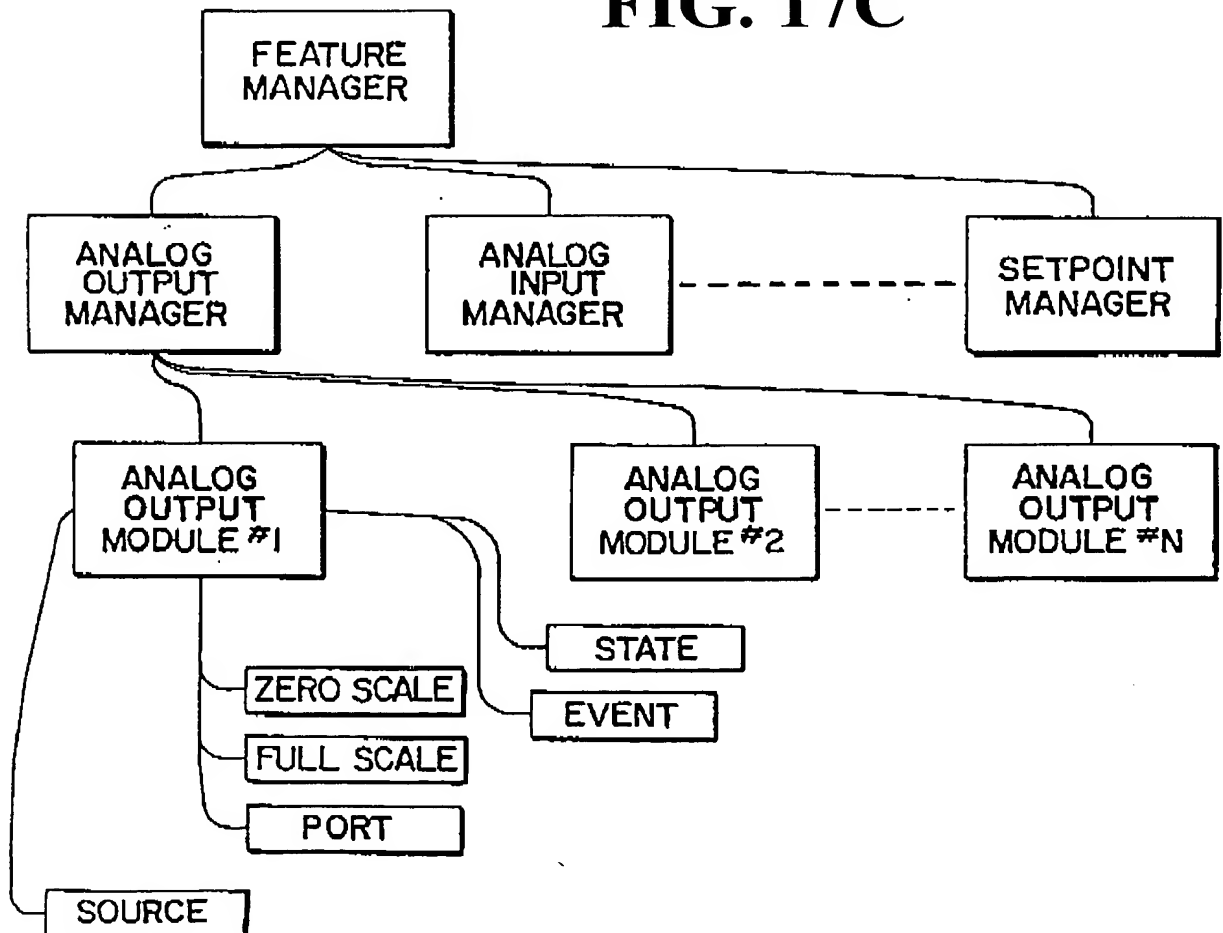


FIG. 18

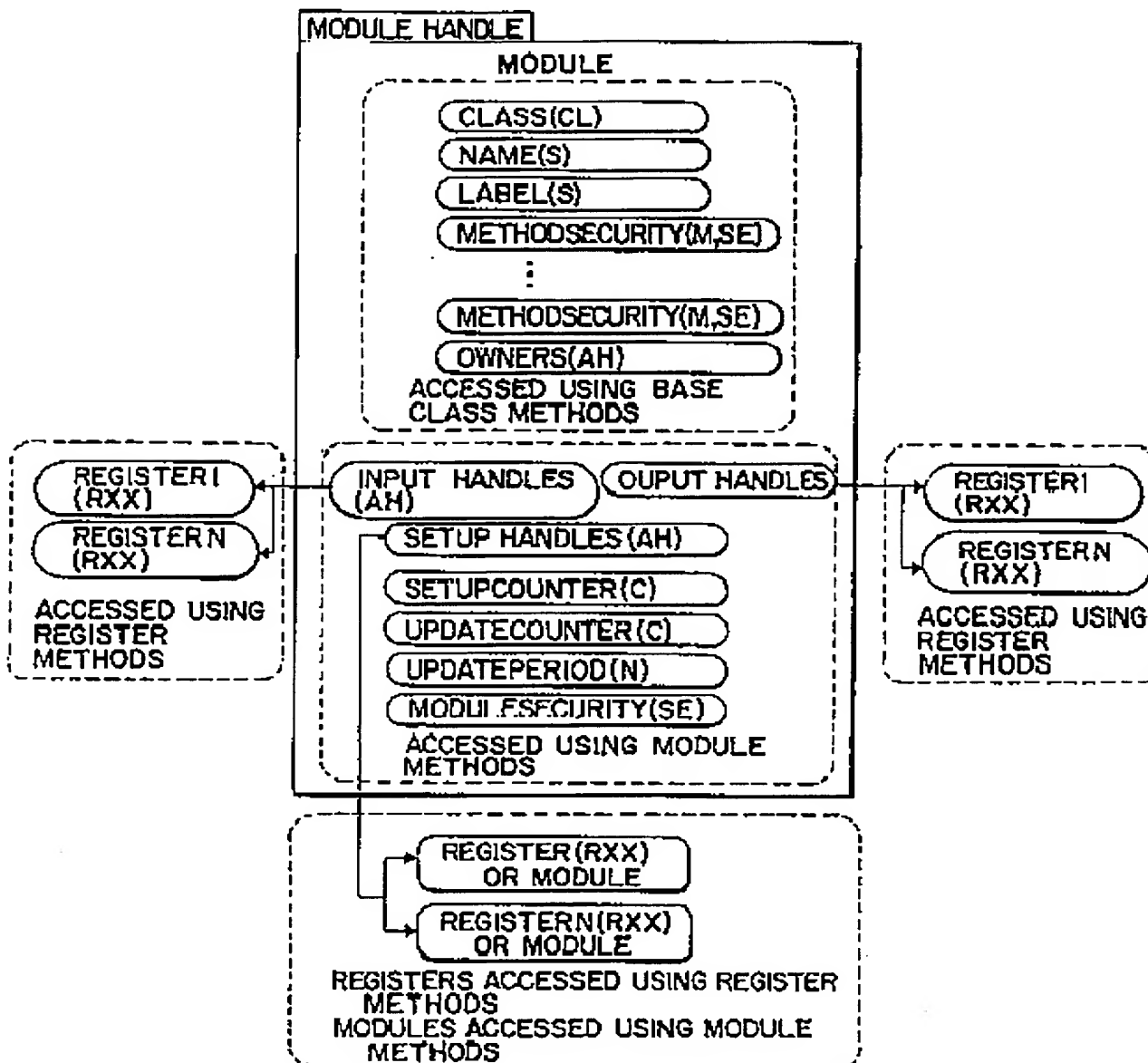


FIG. 19

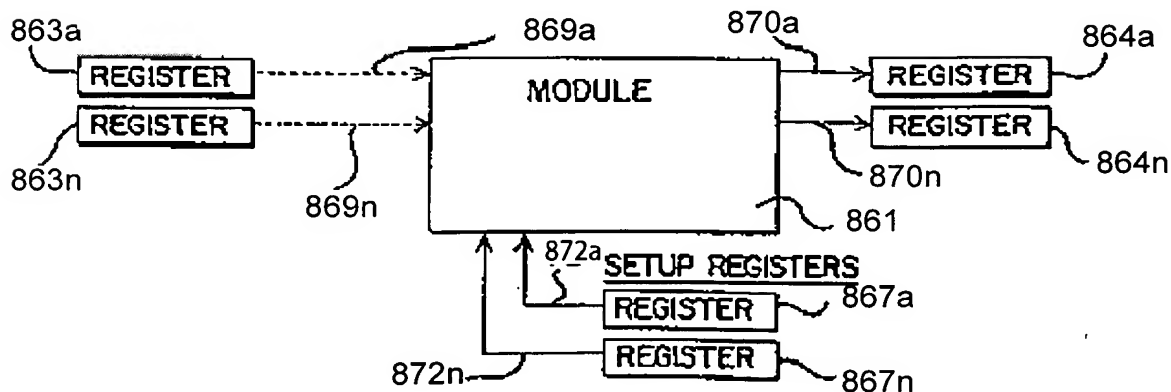


FIG. 19A

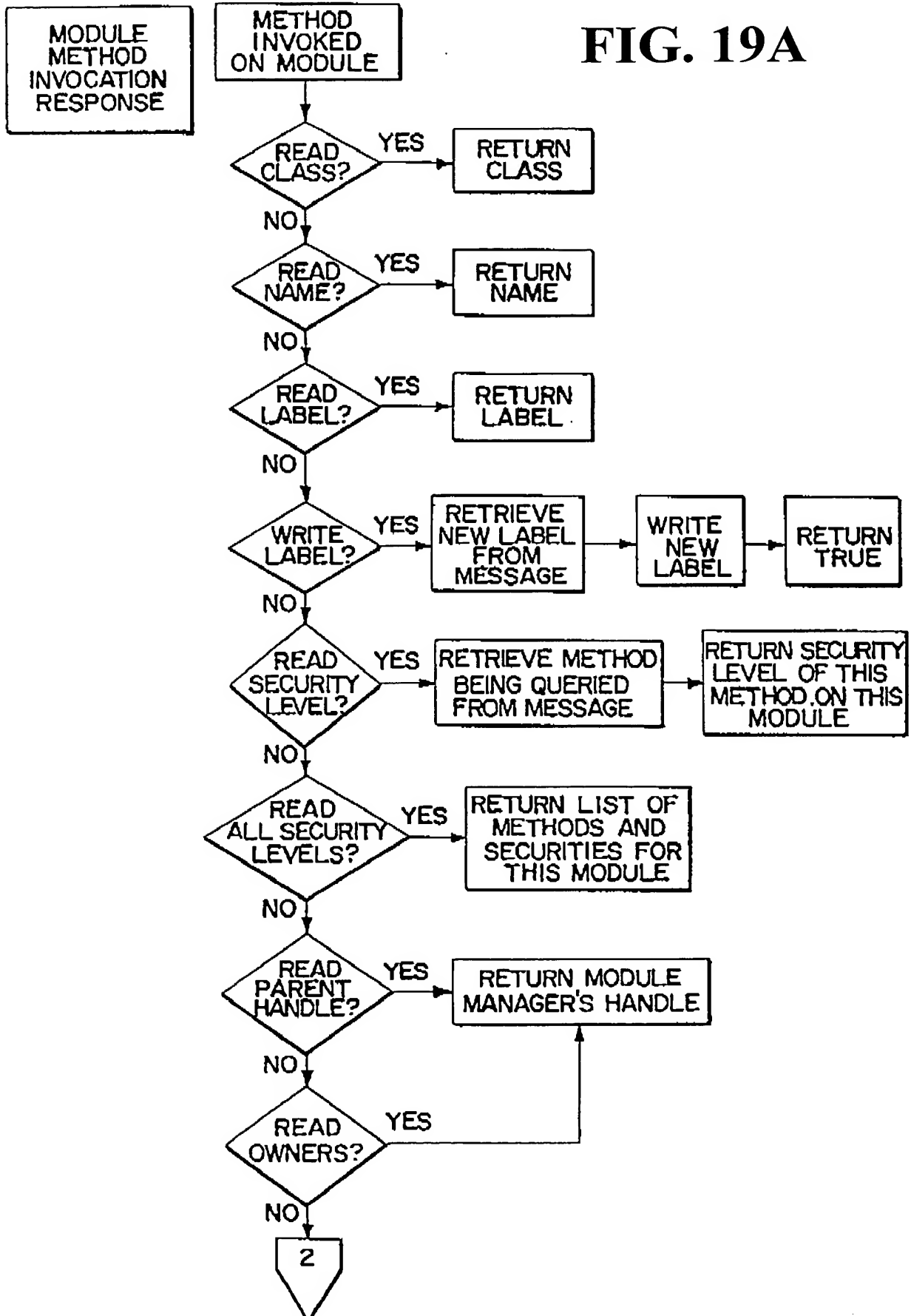


FIG. 19B

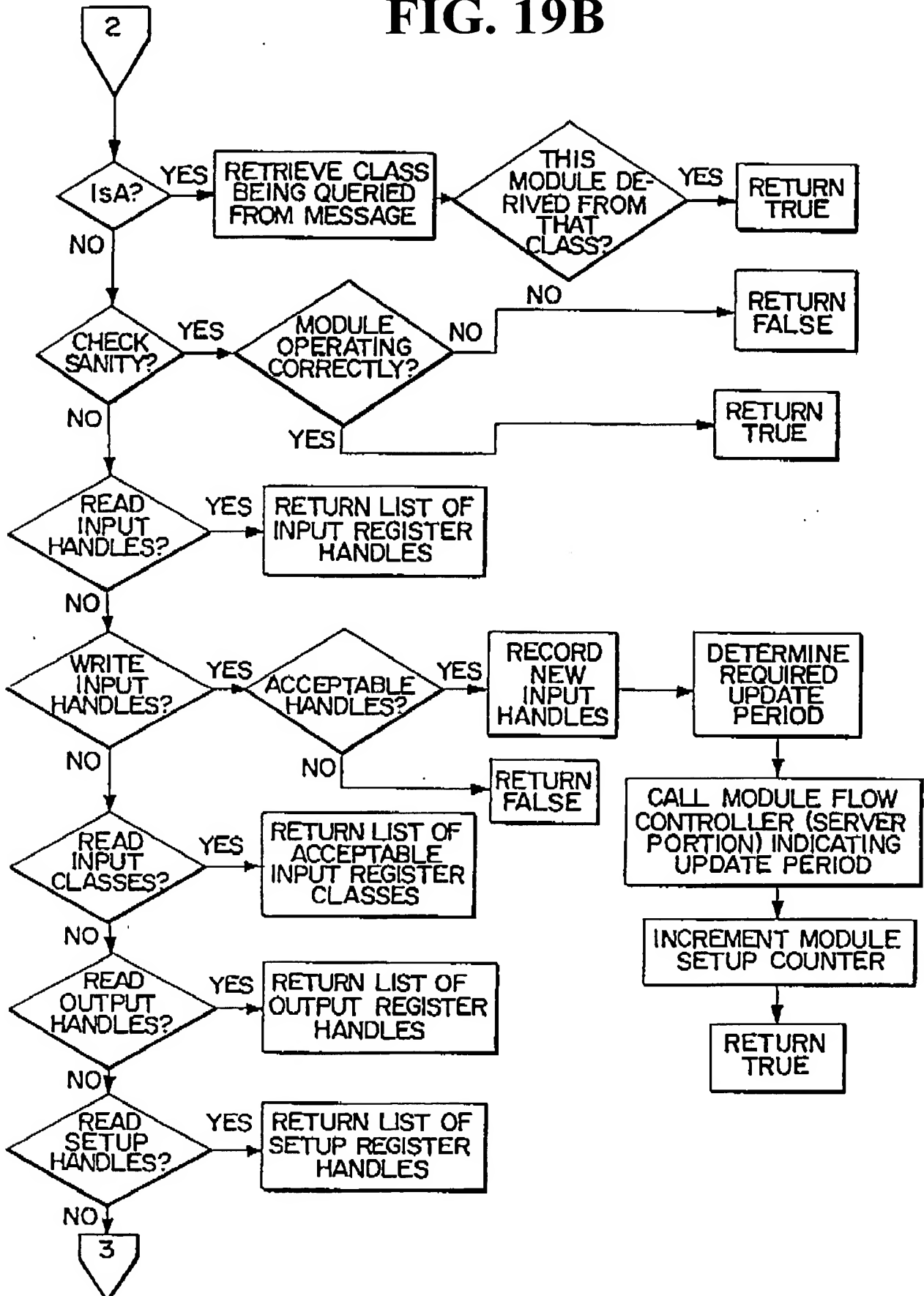


FIG. 19C

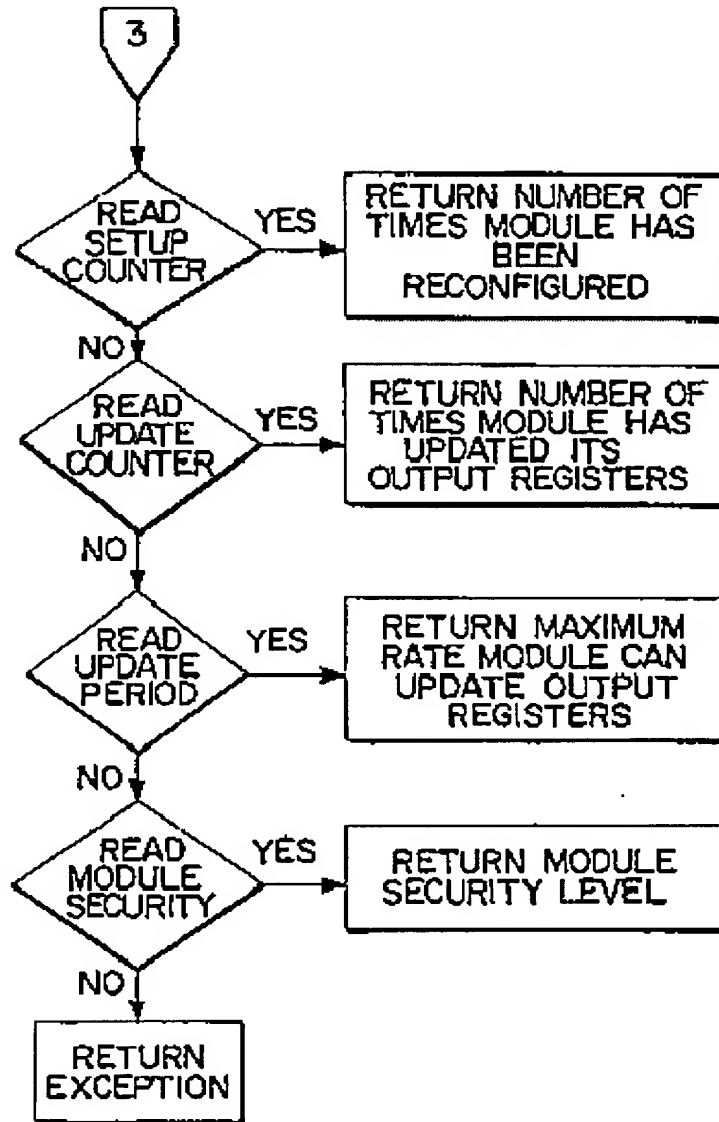


FIG. 20

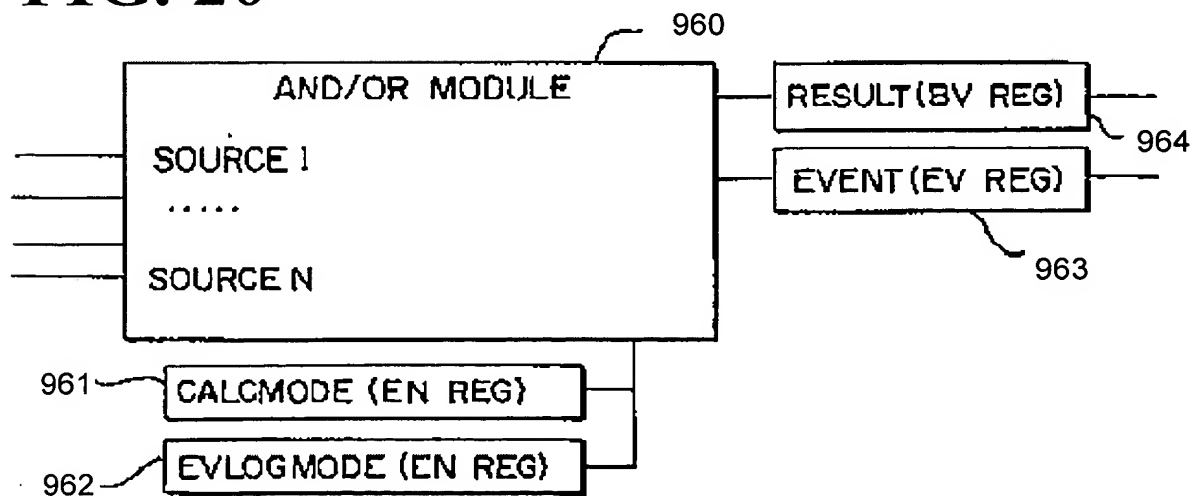


FIG. 20A

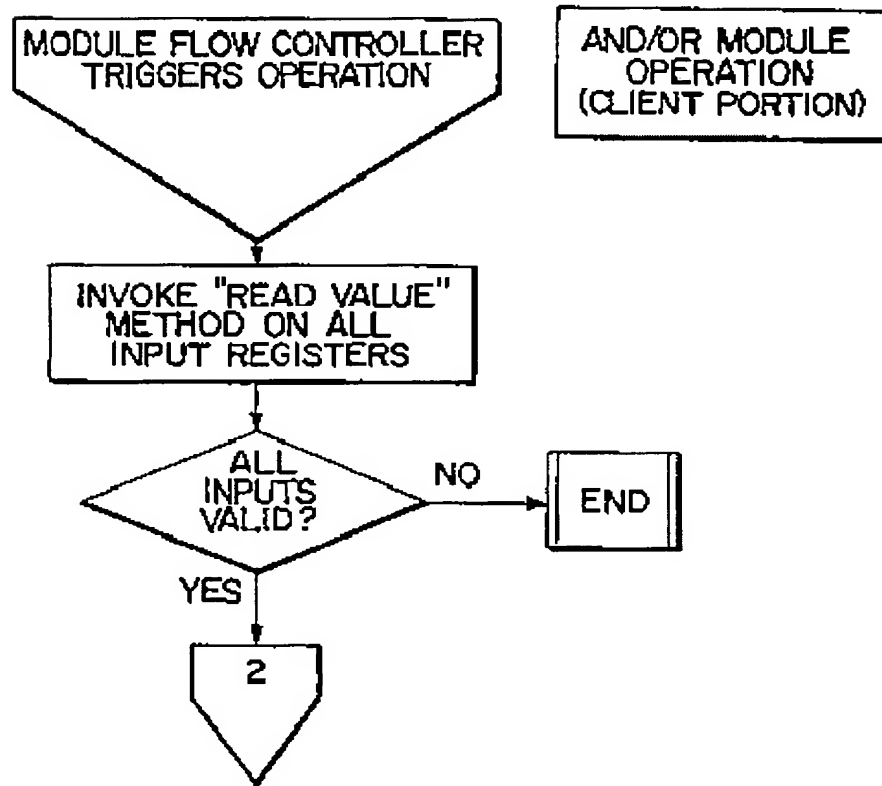


FIG. 21

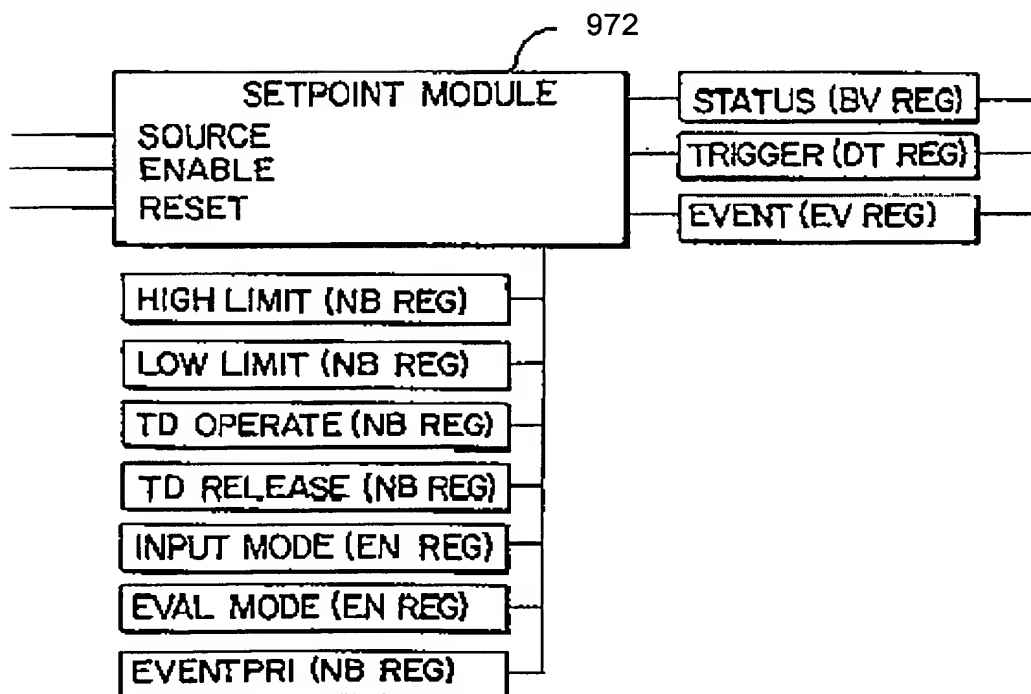


FIG. 20B

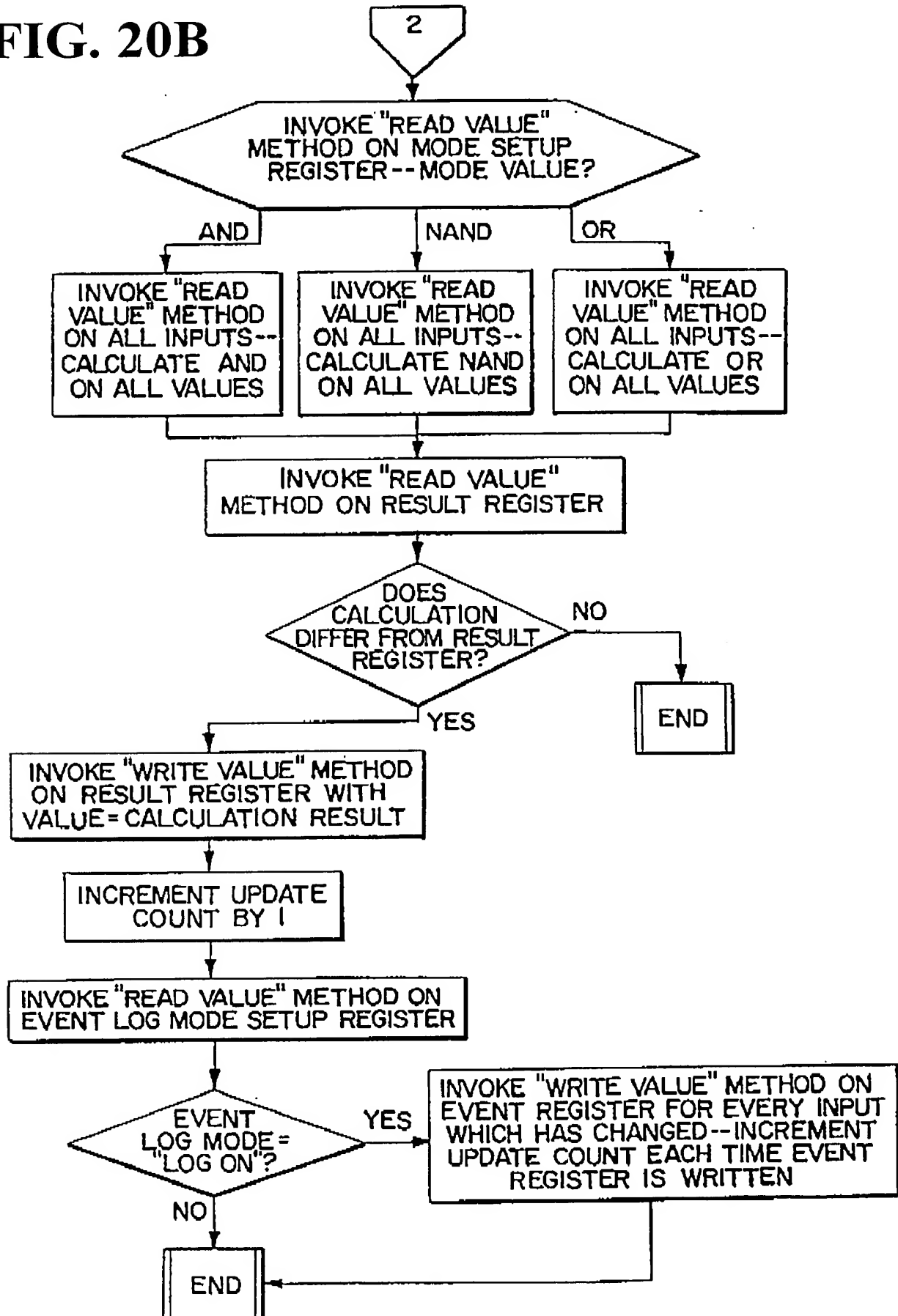


FIG. 21A

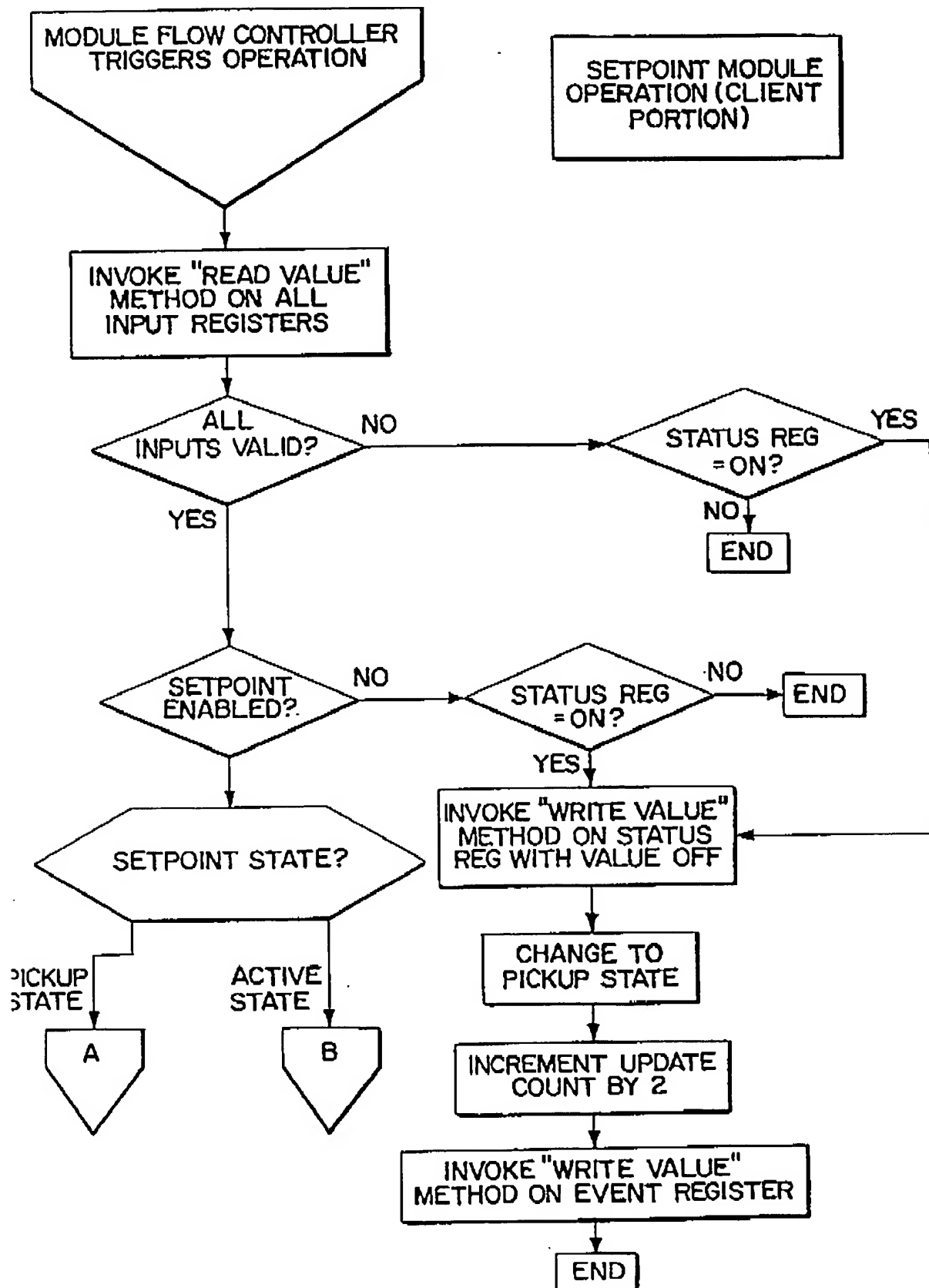


FIG. 21B

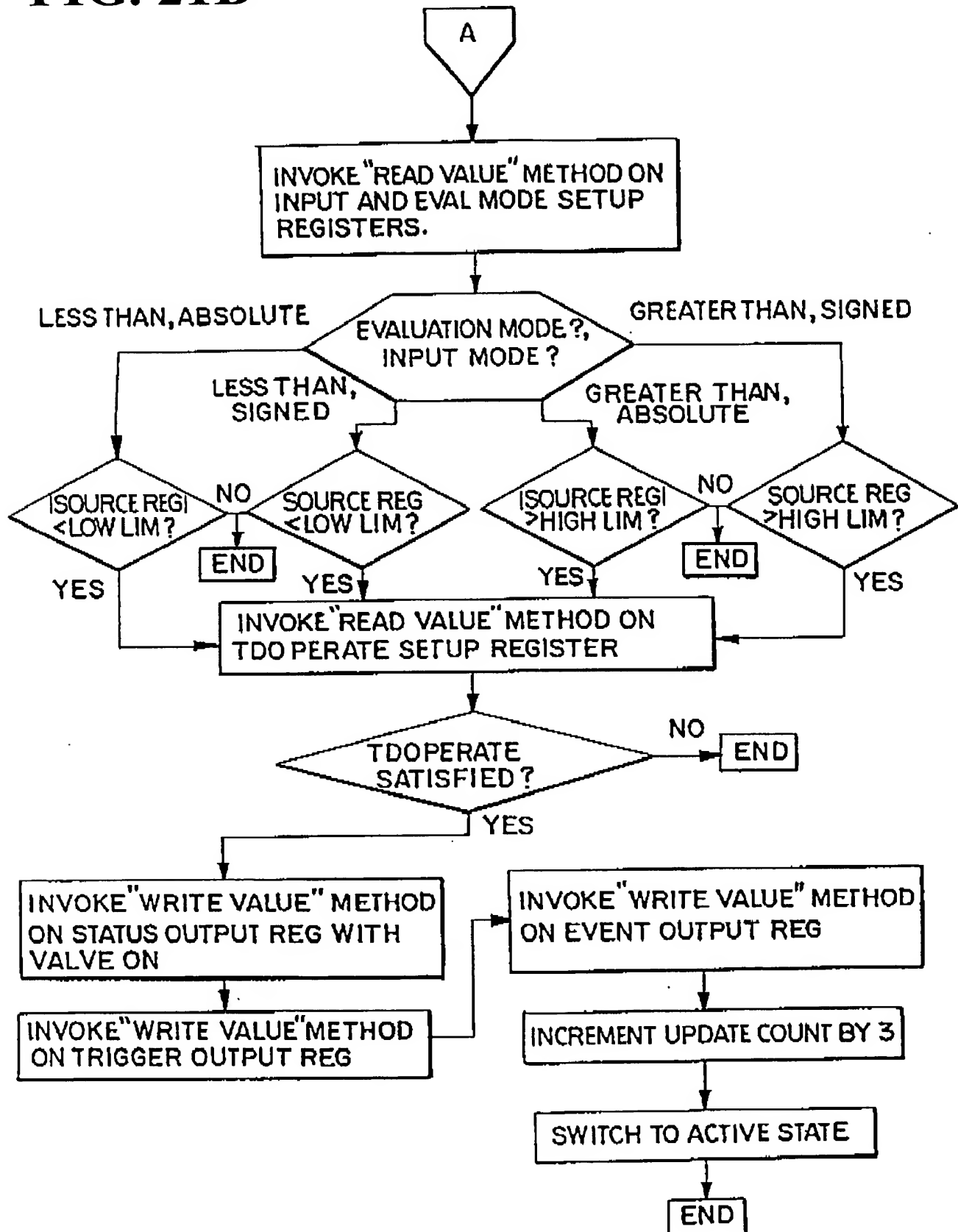


FIG. 21C

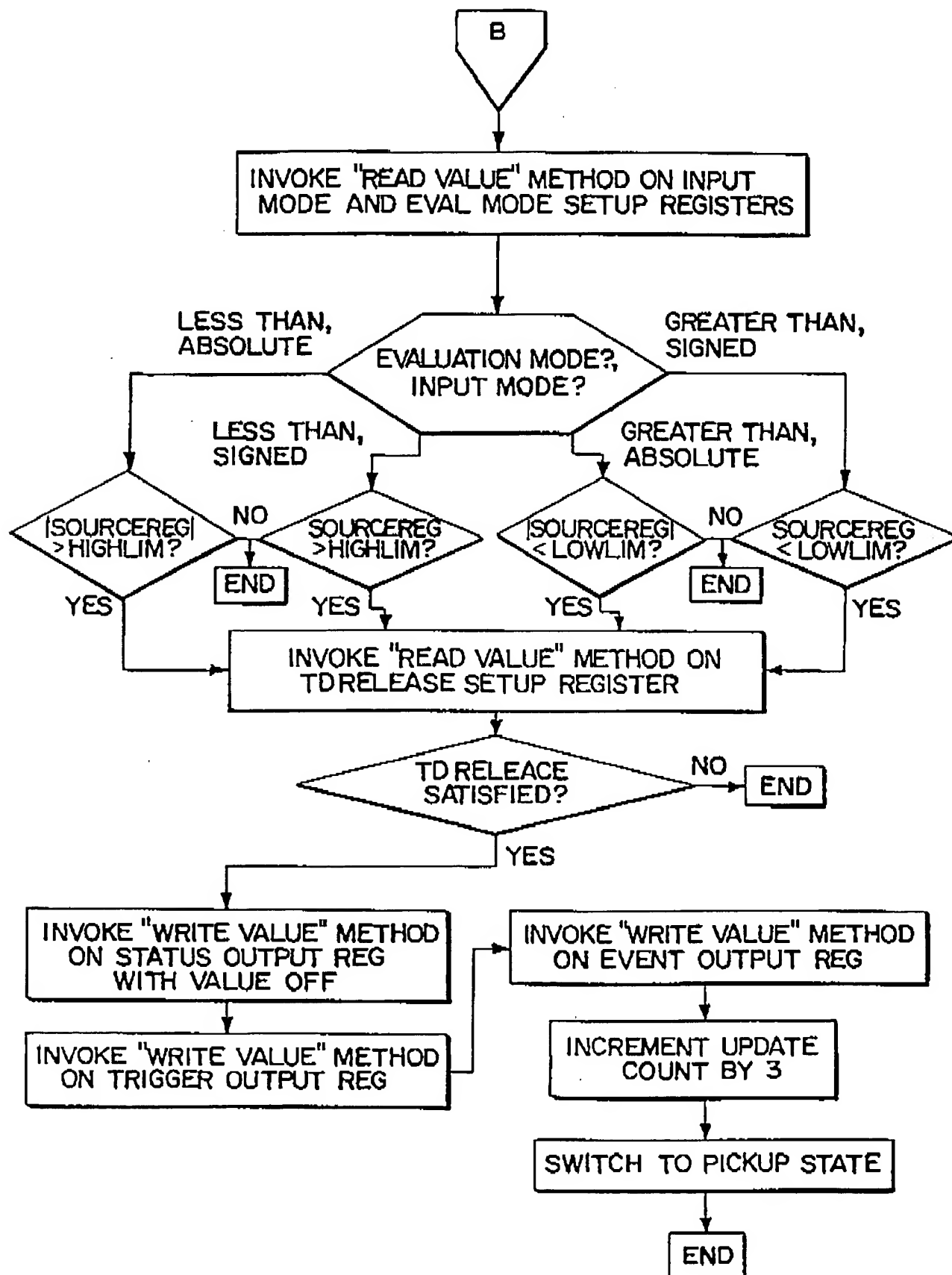


FIG. 22A

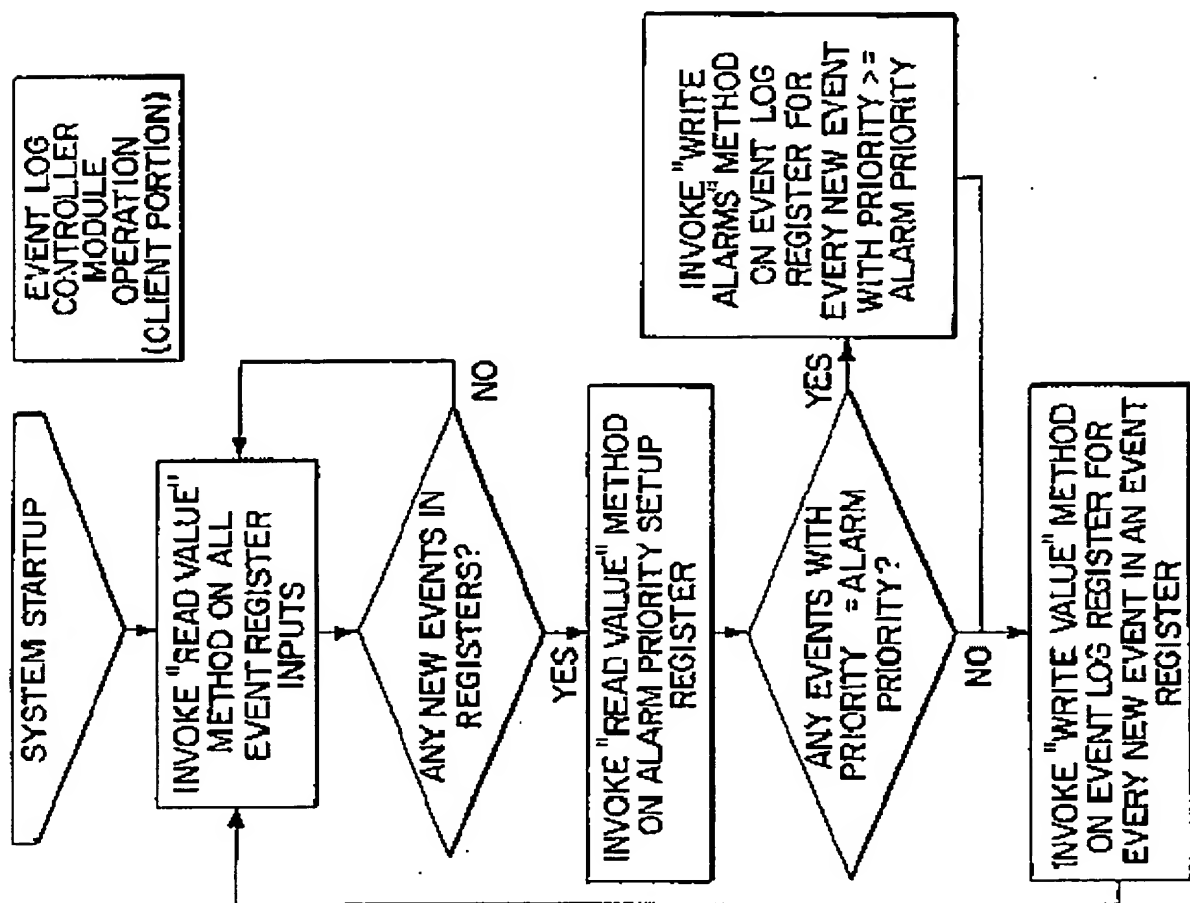


FIG. 22

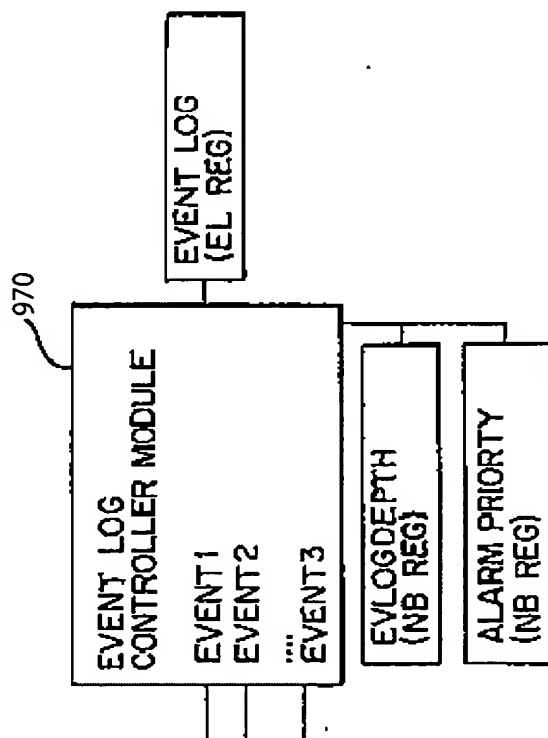


FIG. 24A

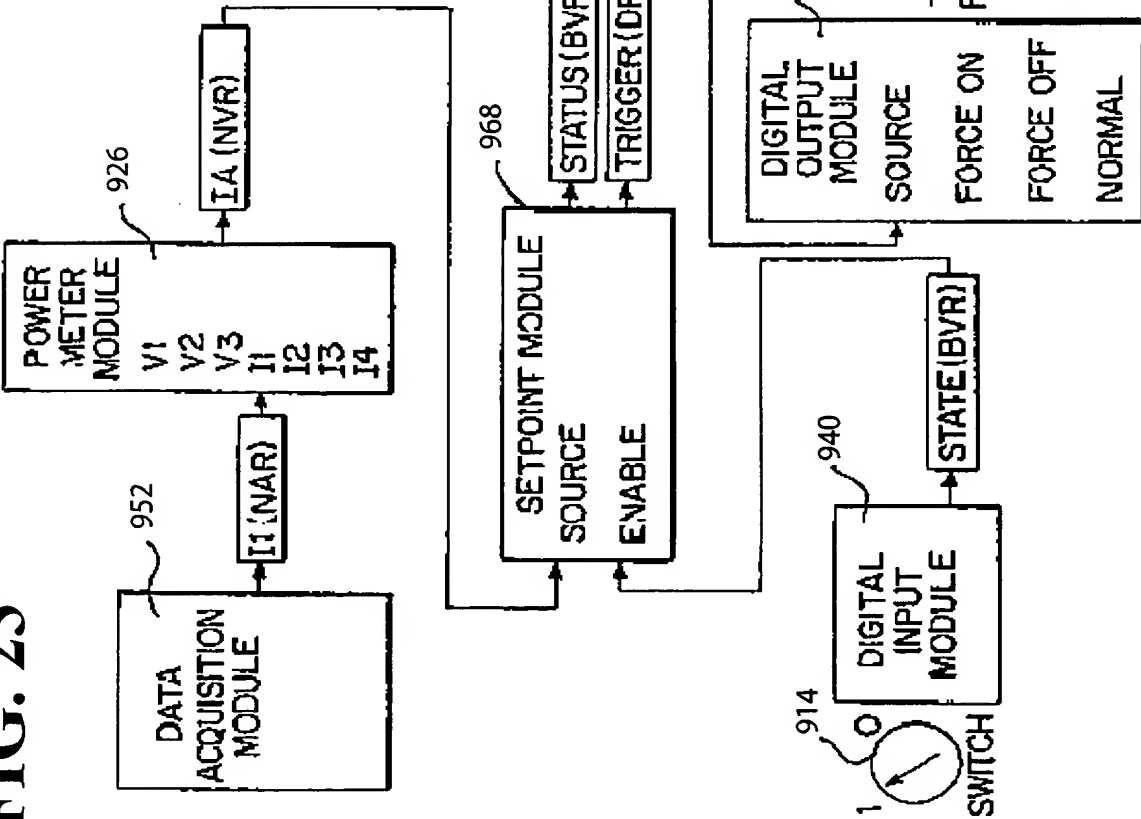


FIG. 25

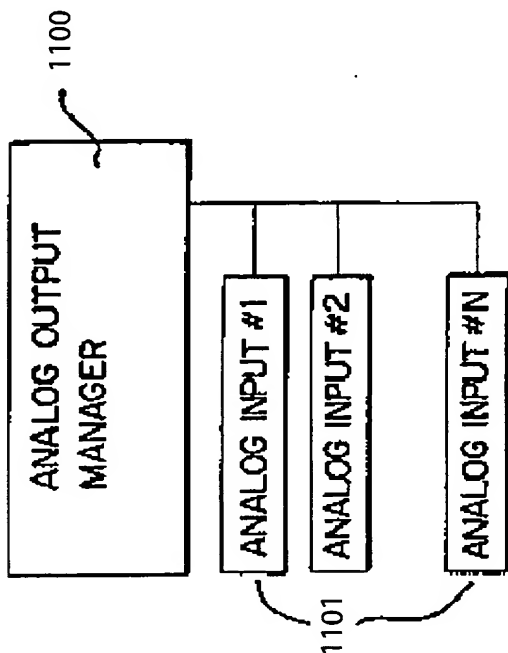


FIG. 24B

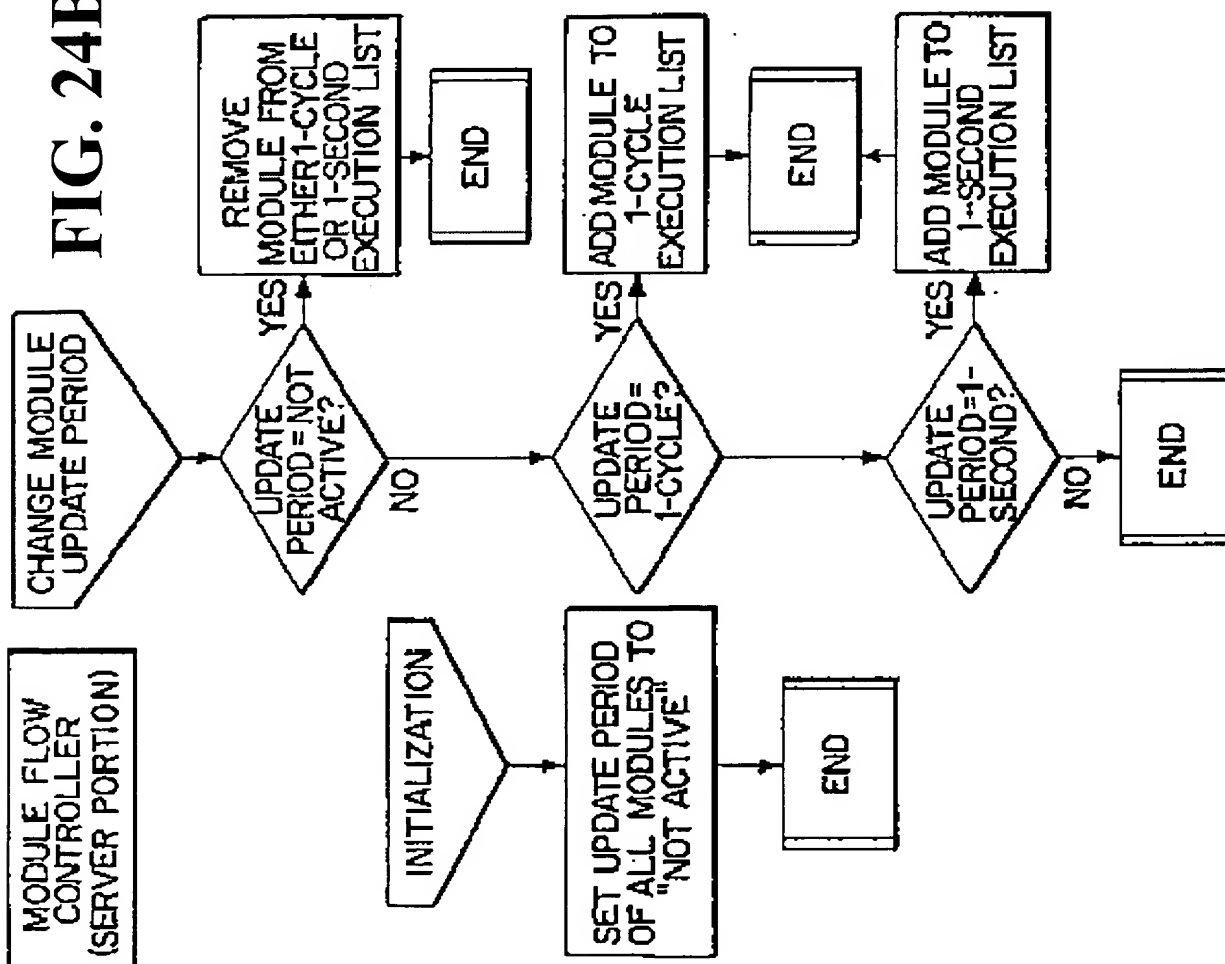


FIG. 25A

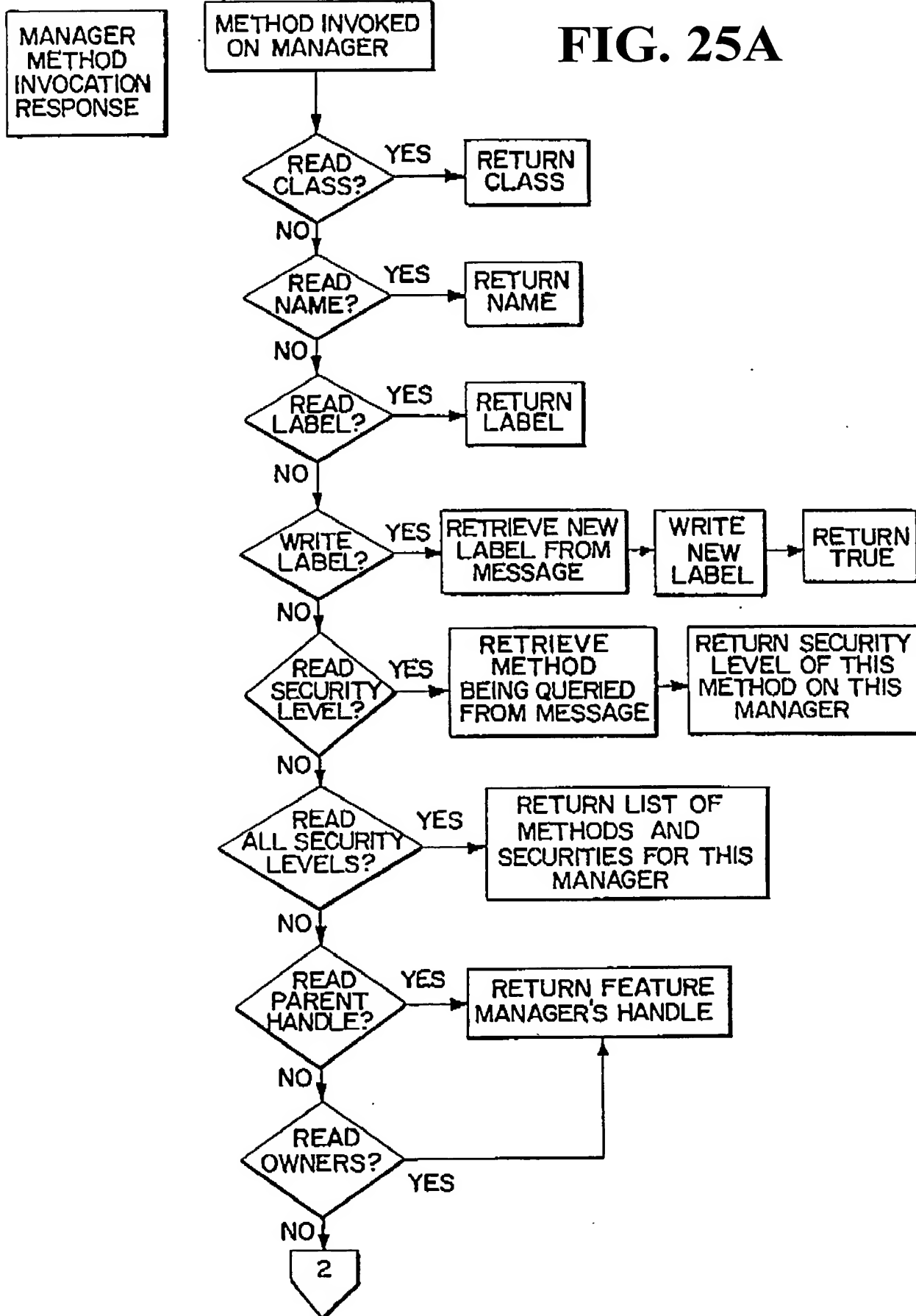


FIG. 25B

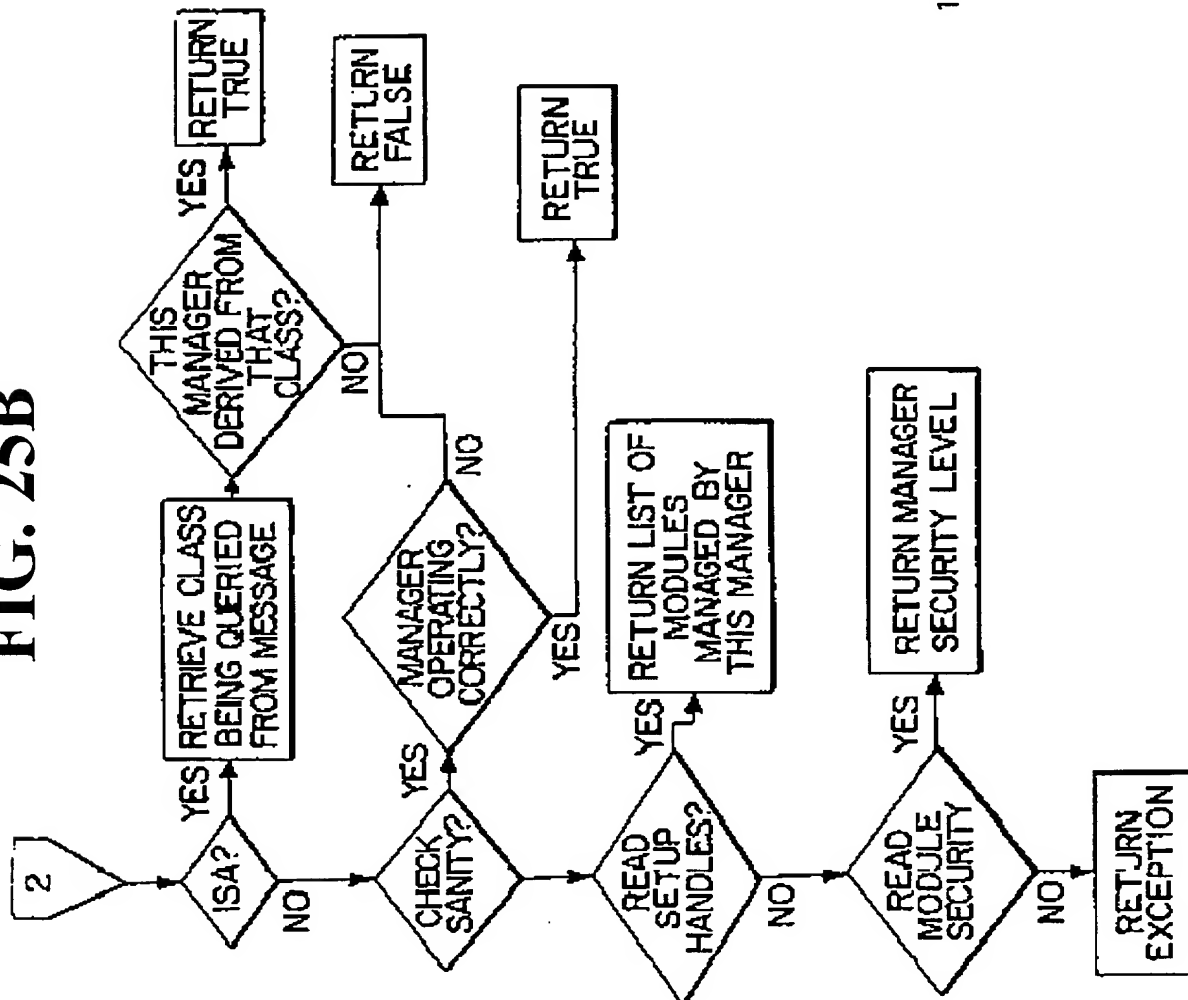
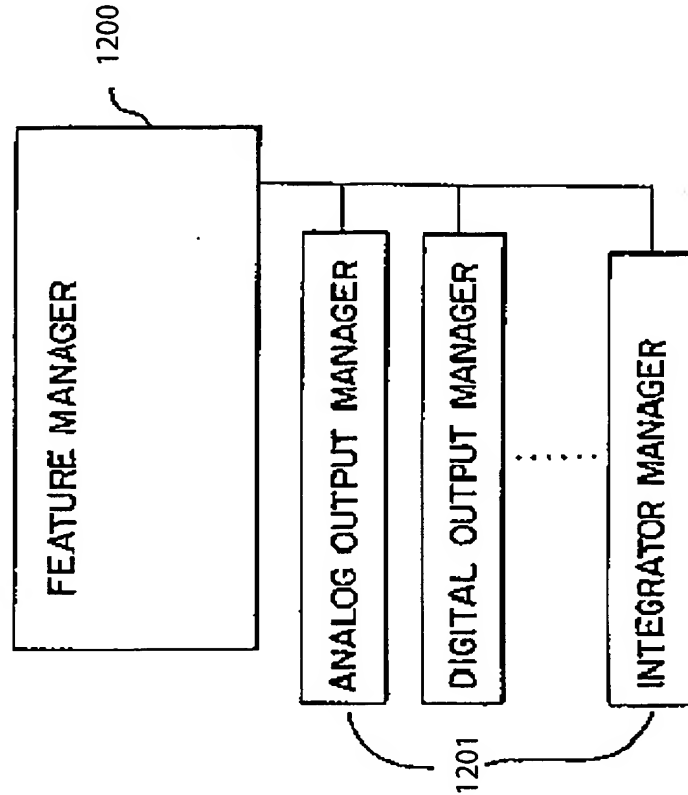


FIG. 26



FEATURE
MANAGER
METHOD
INVOCATION
RESPONSE

FIG. 26A

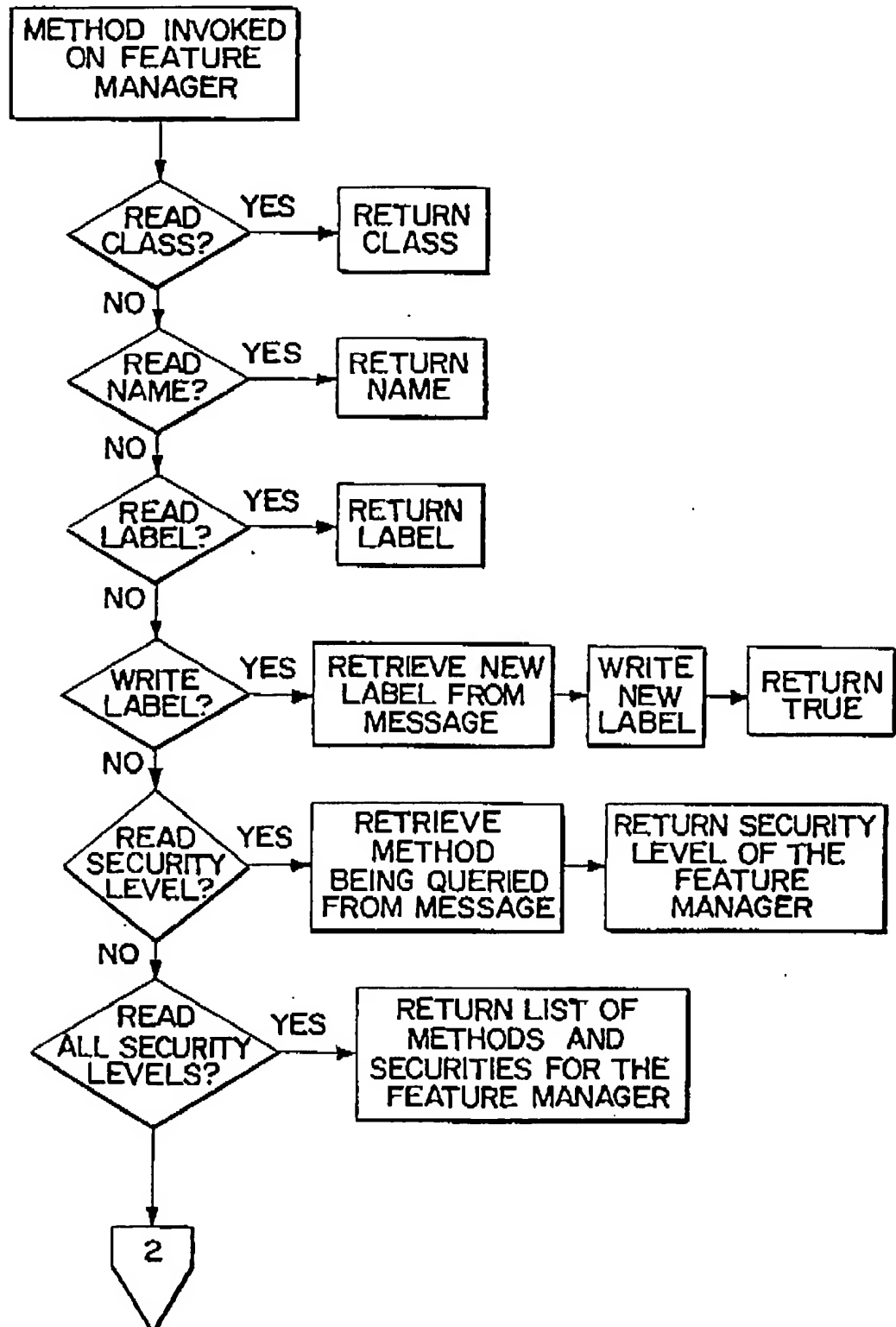
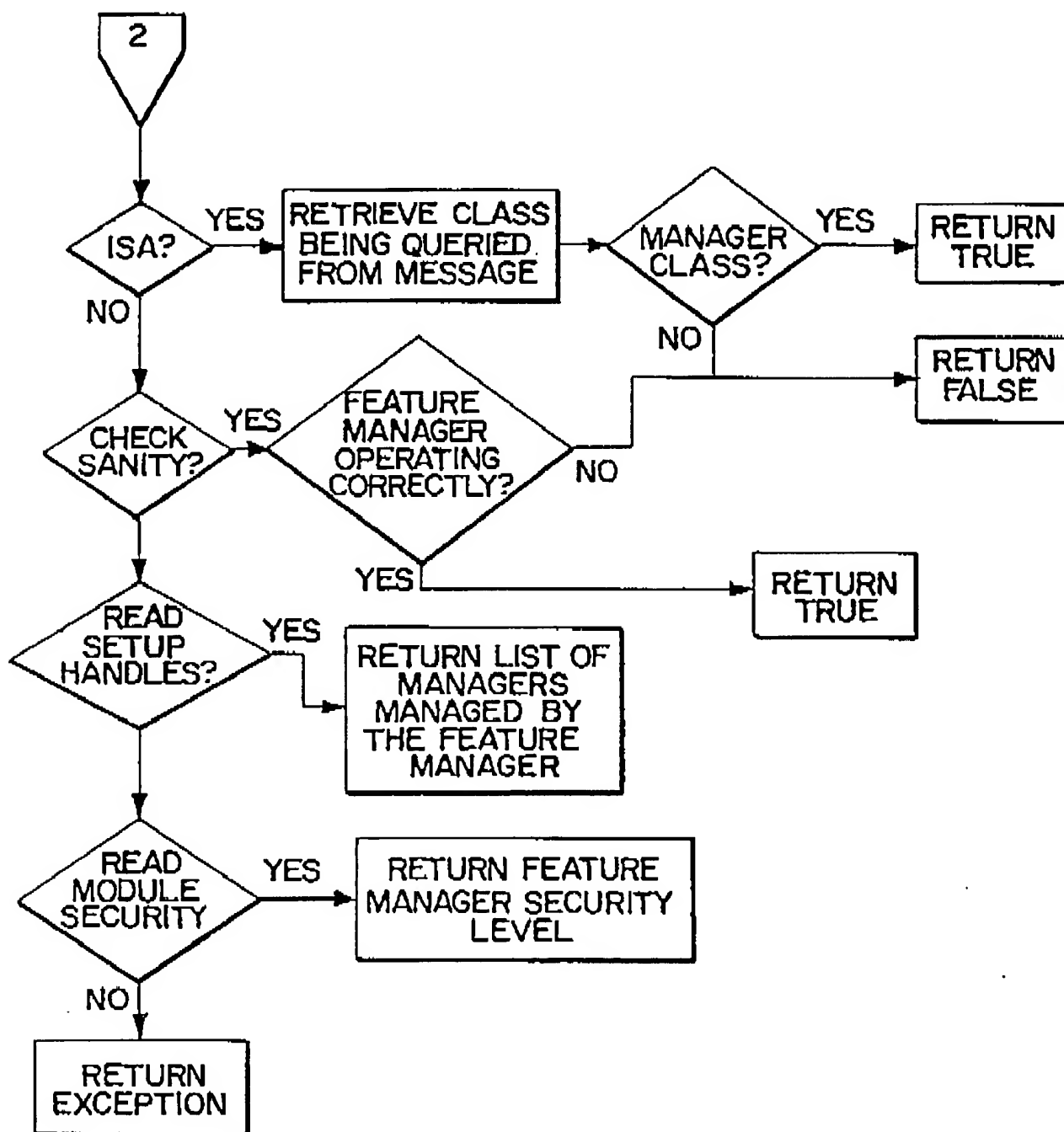


FIG. 26B



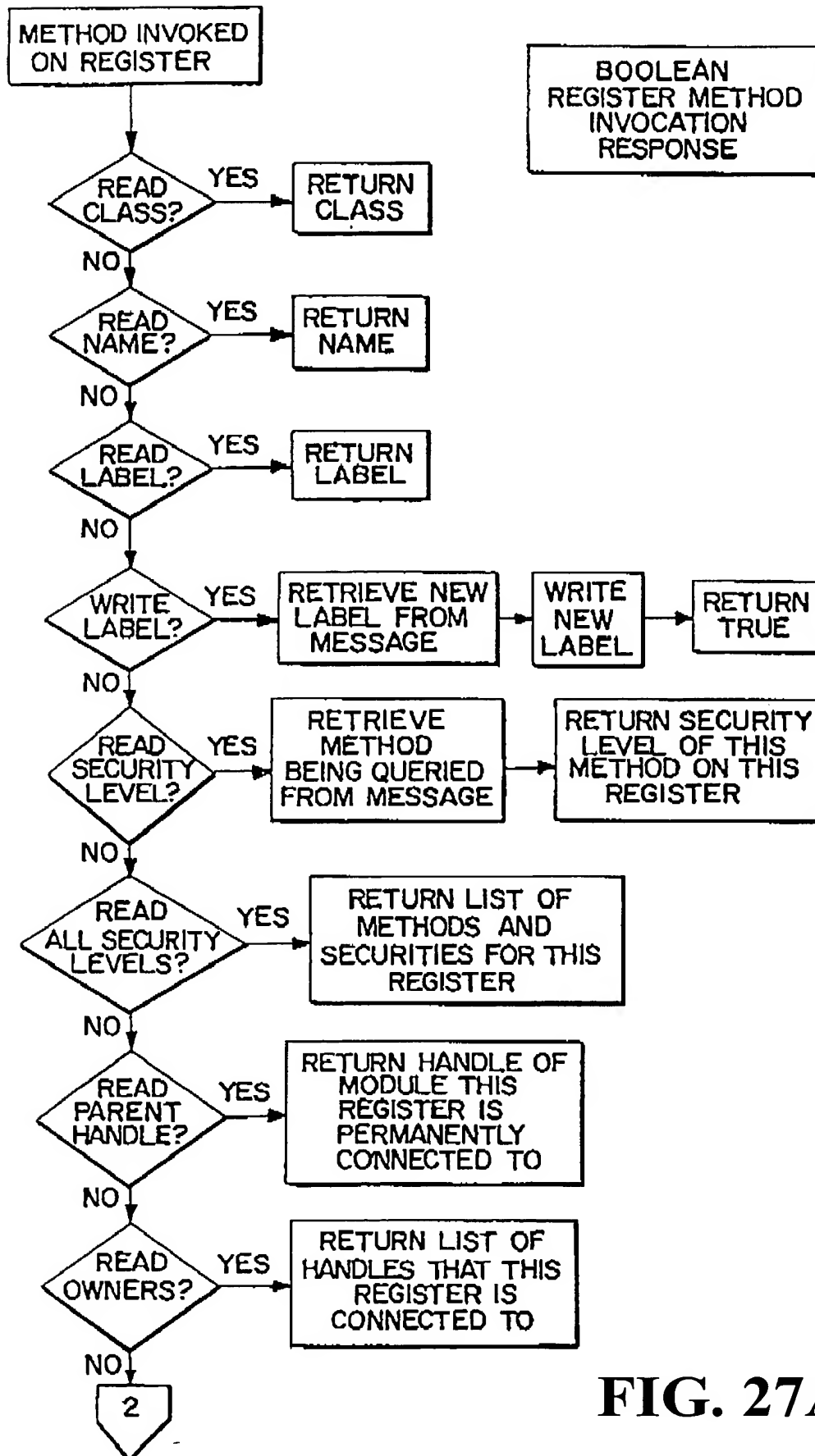


FIG. 27A

FIG. 27B

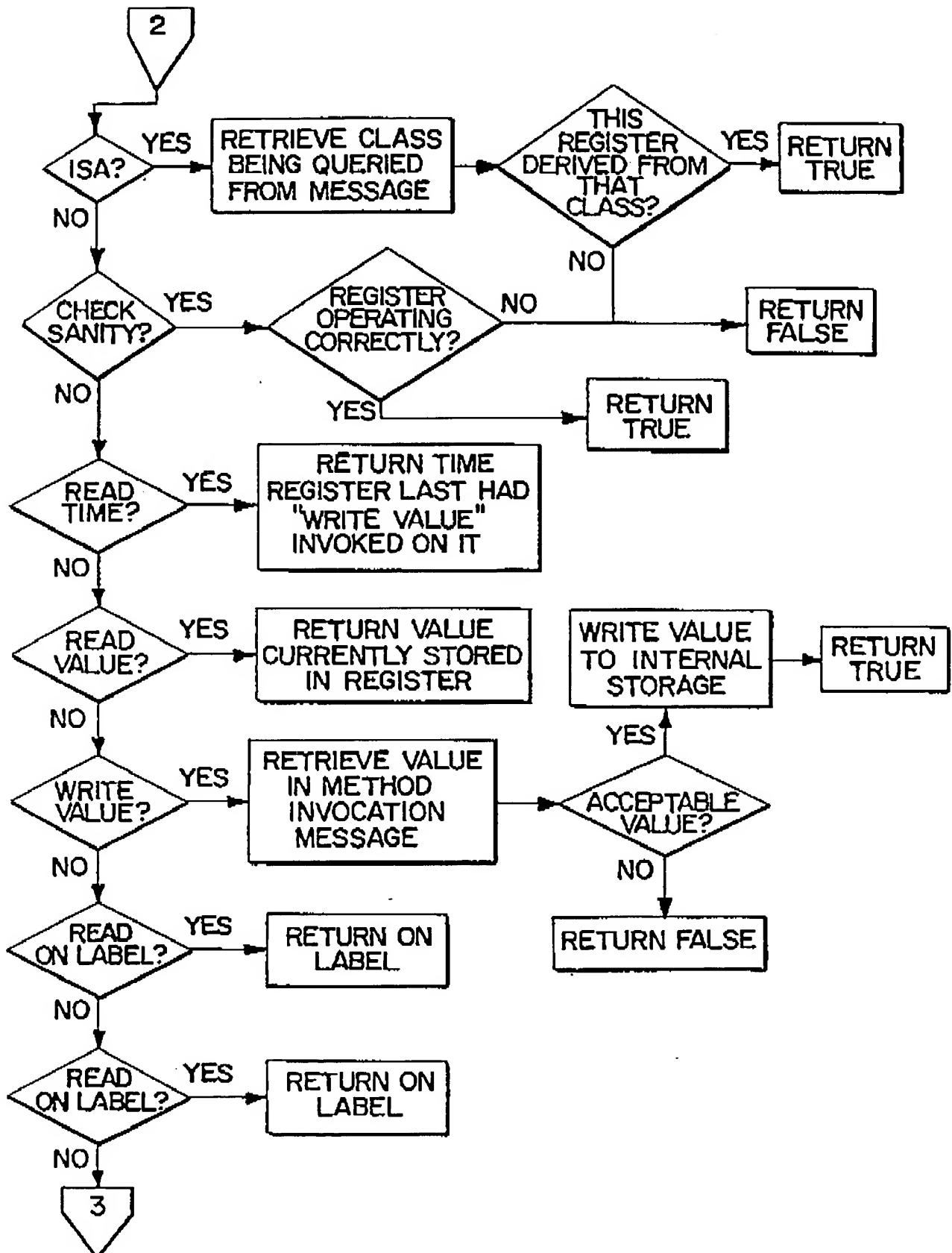


FIG. 27C

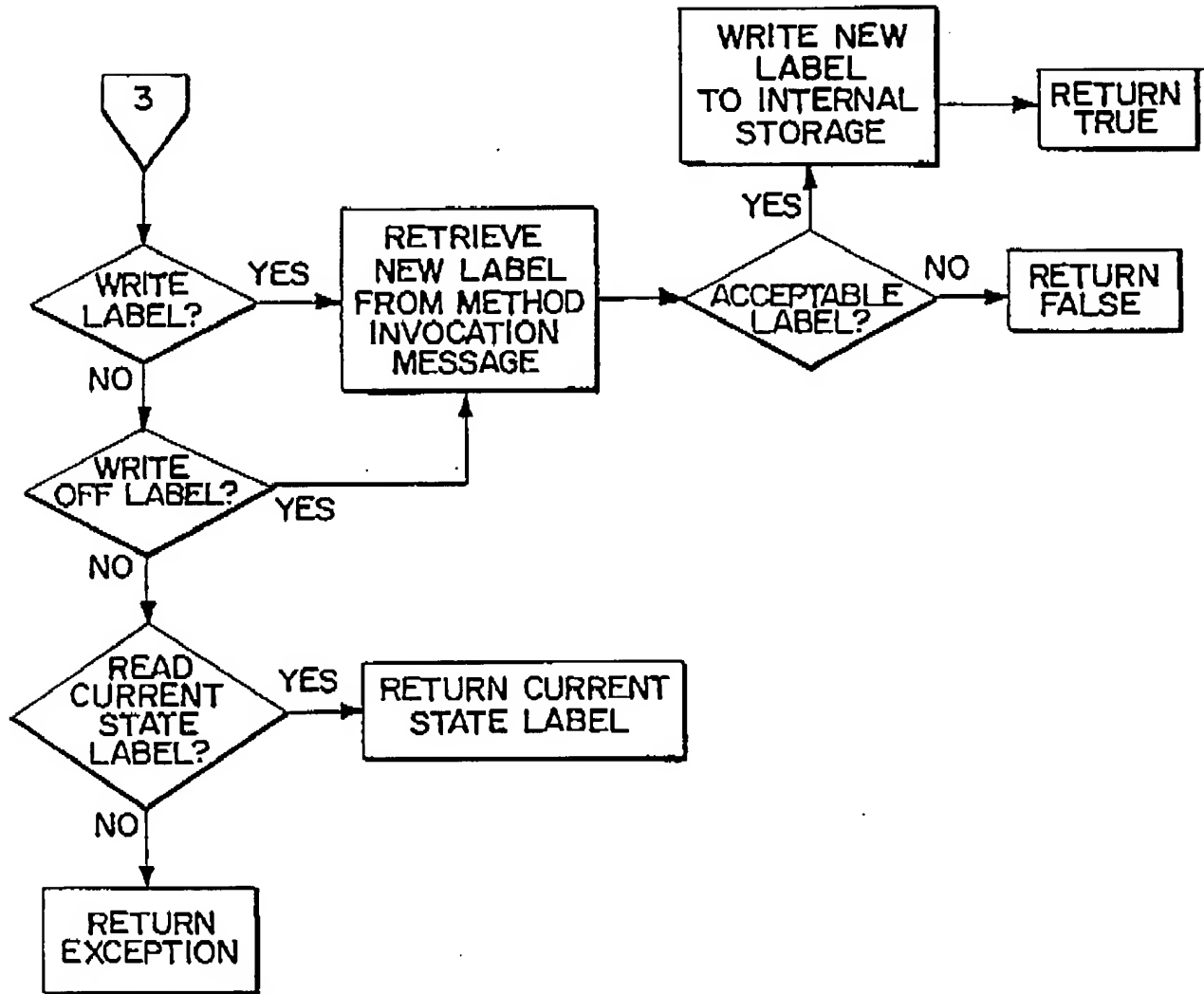


FIG. 28A

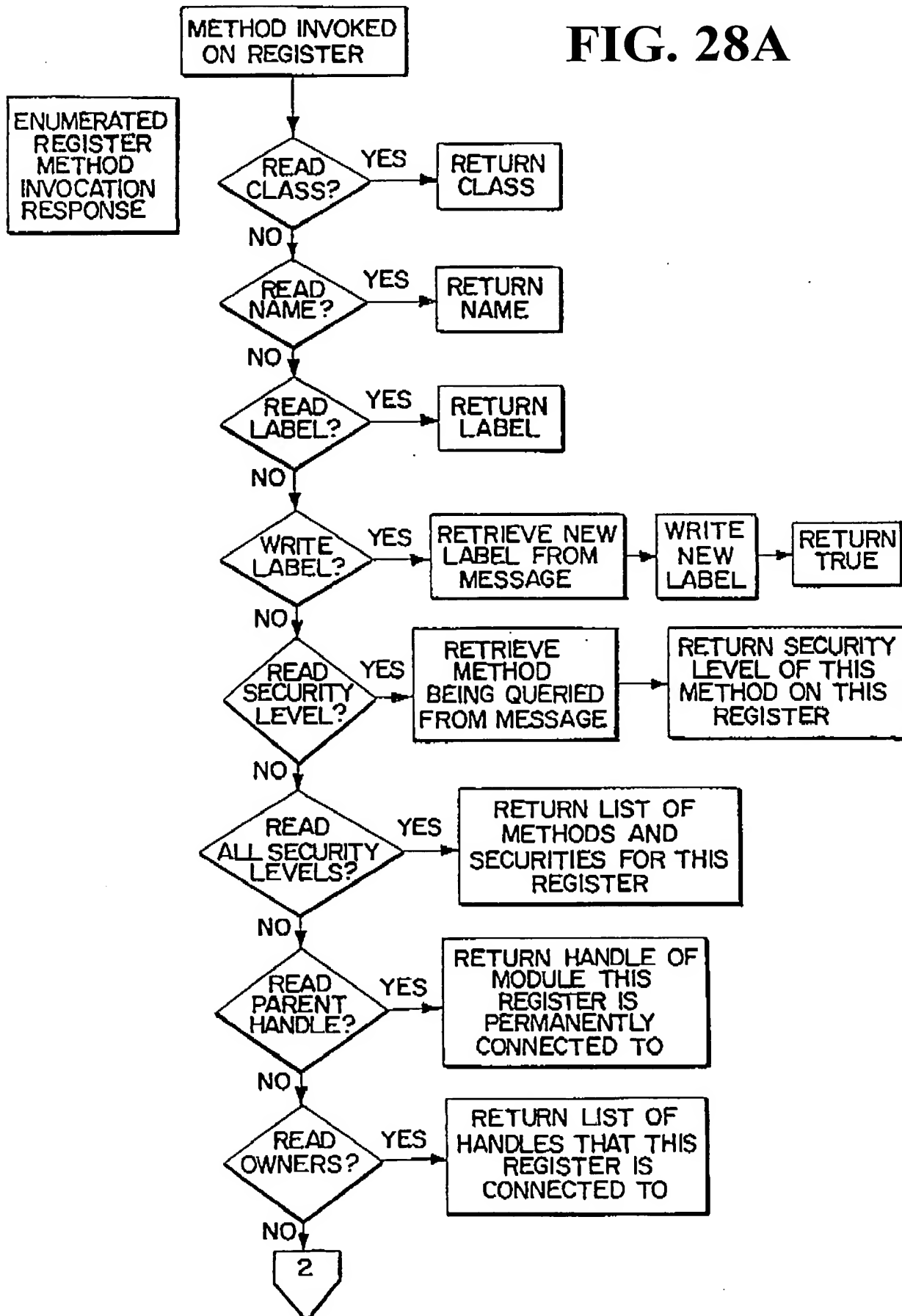


FIG. 28B

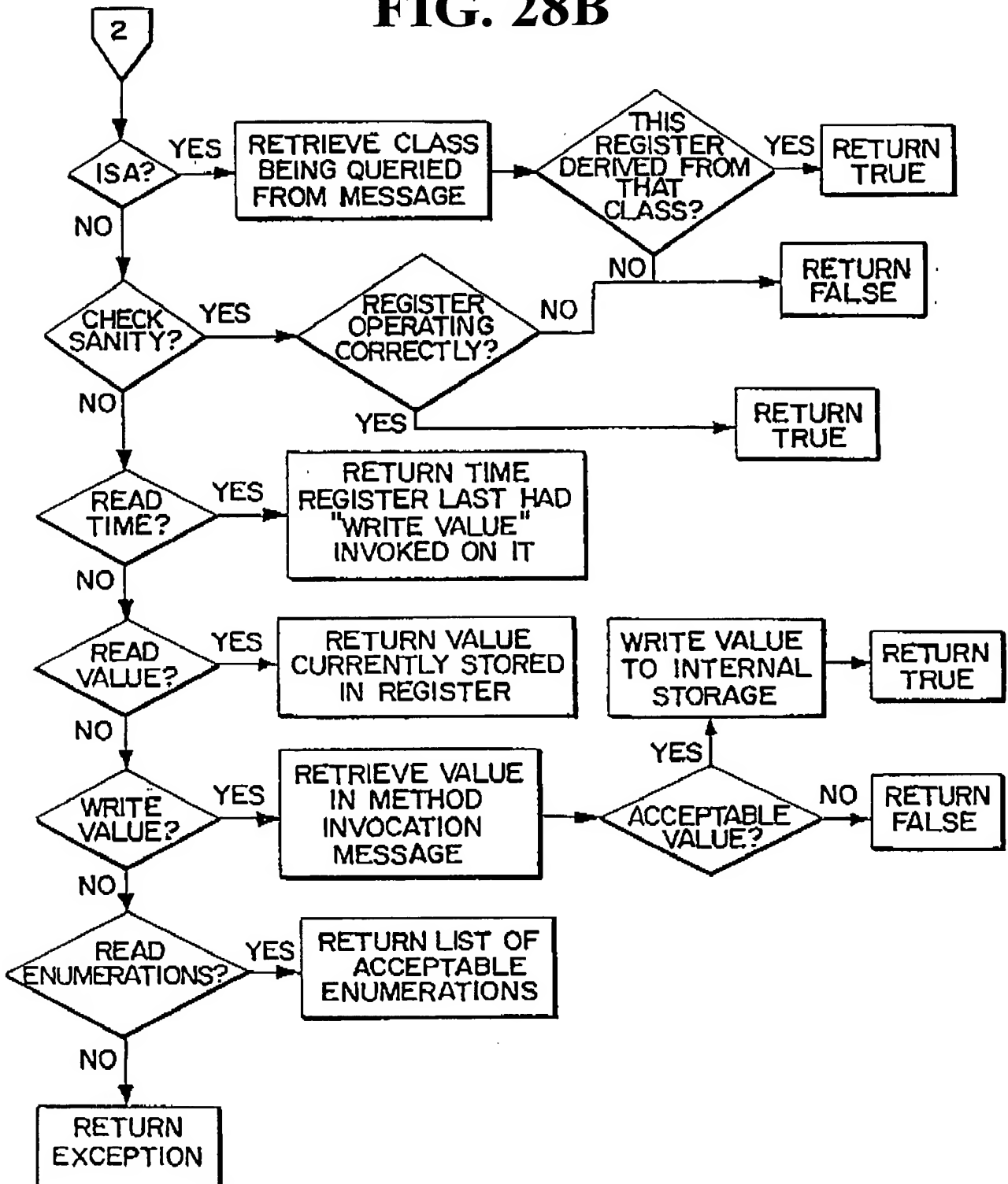


FIG. 29A

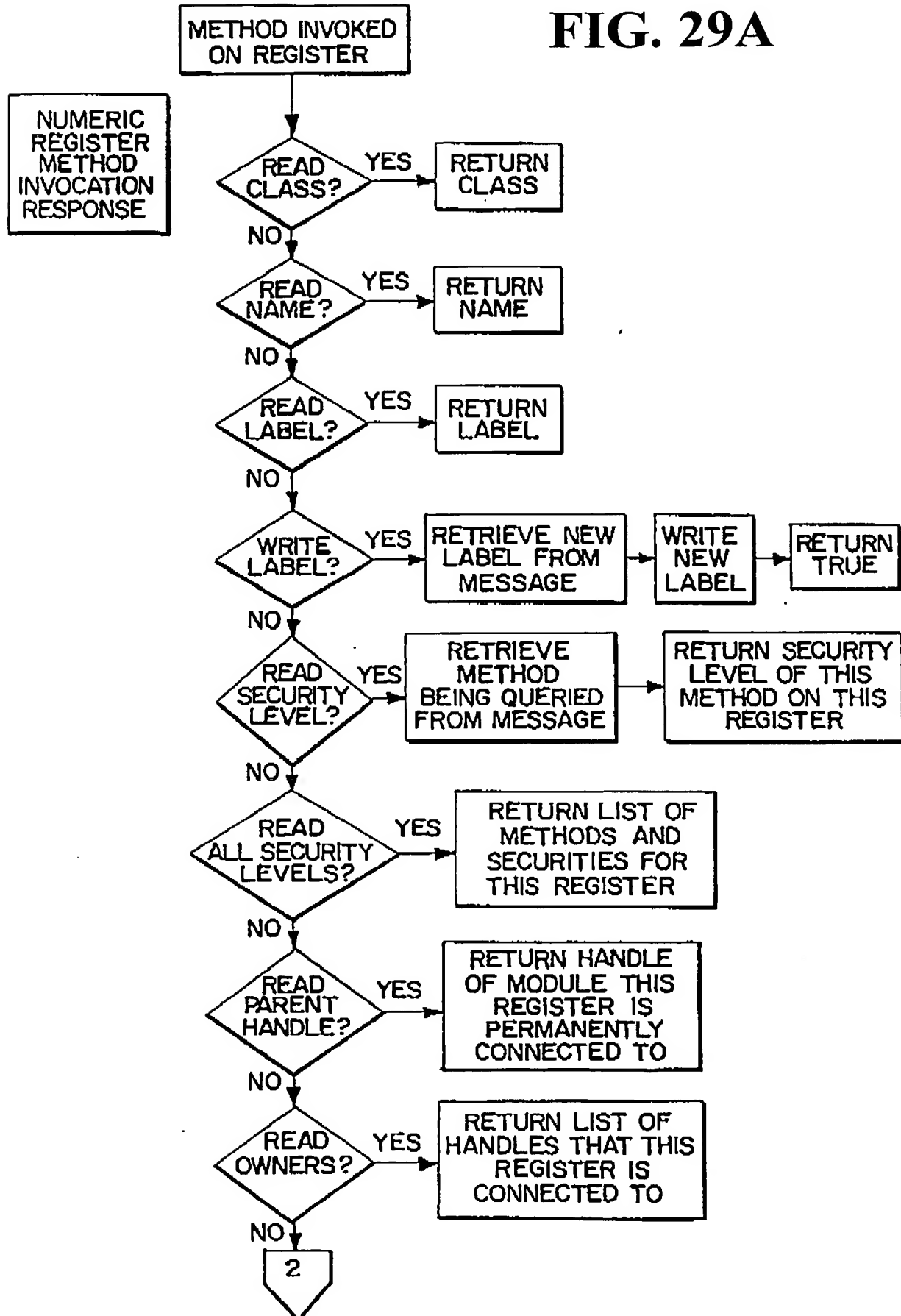


FIG. 29B

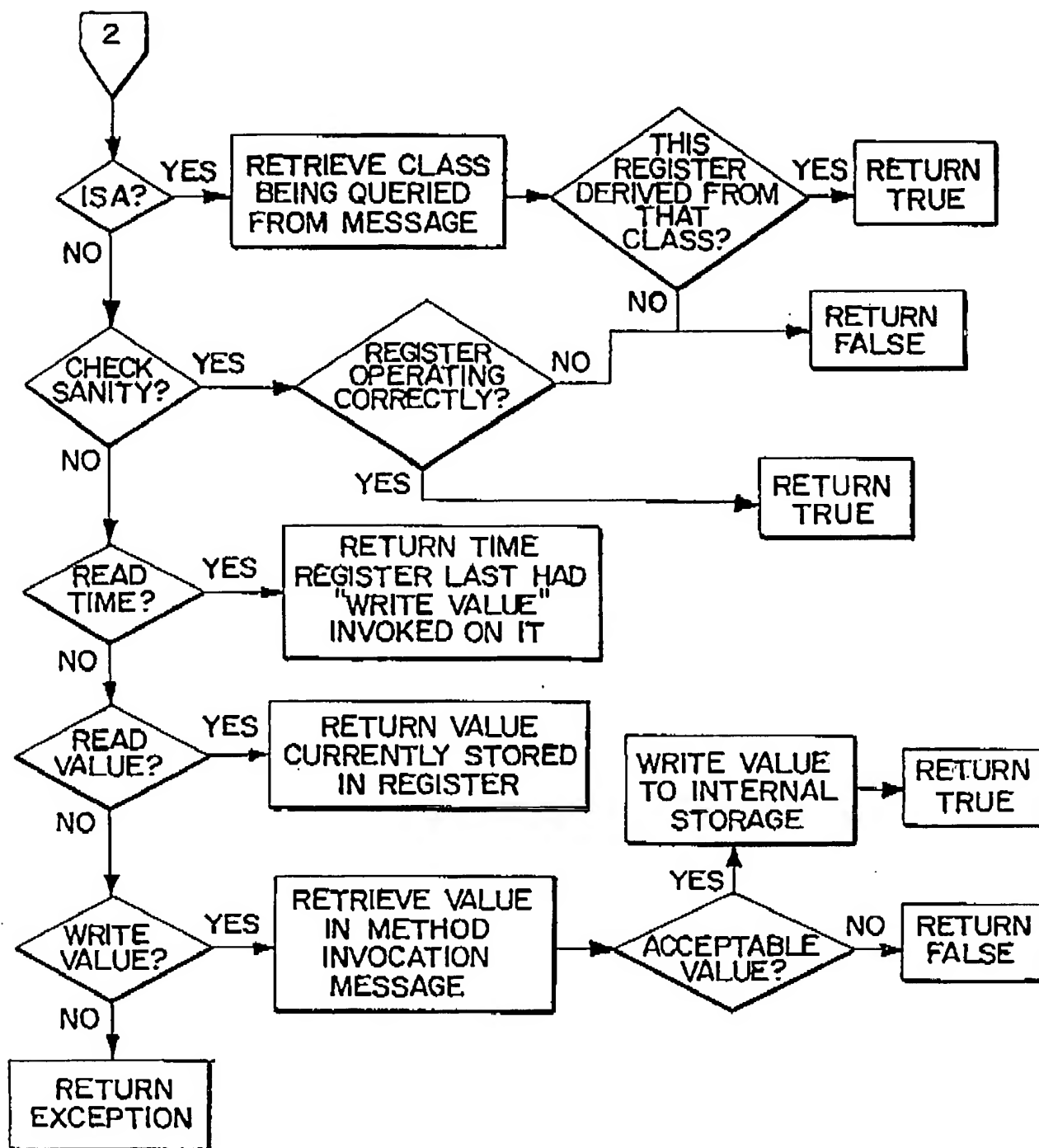


FIG. 30A

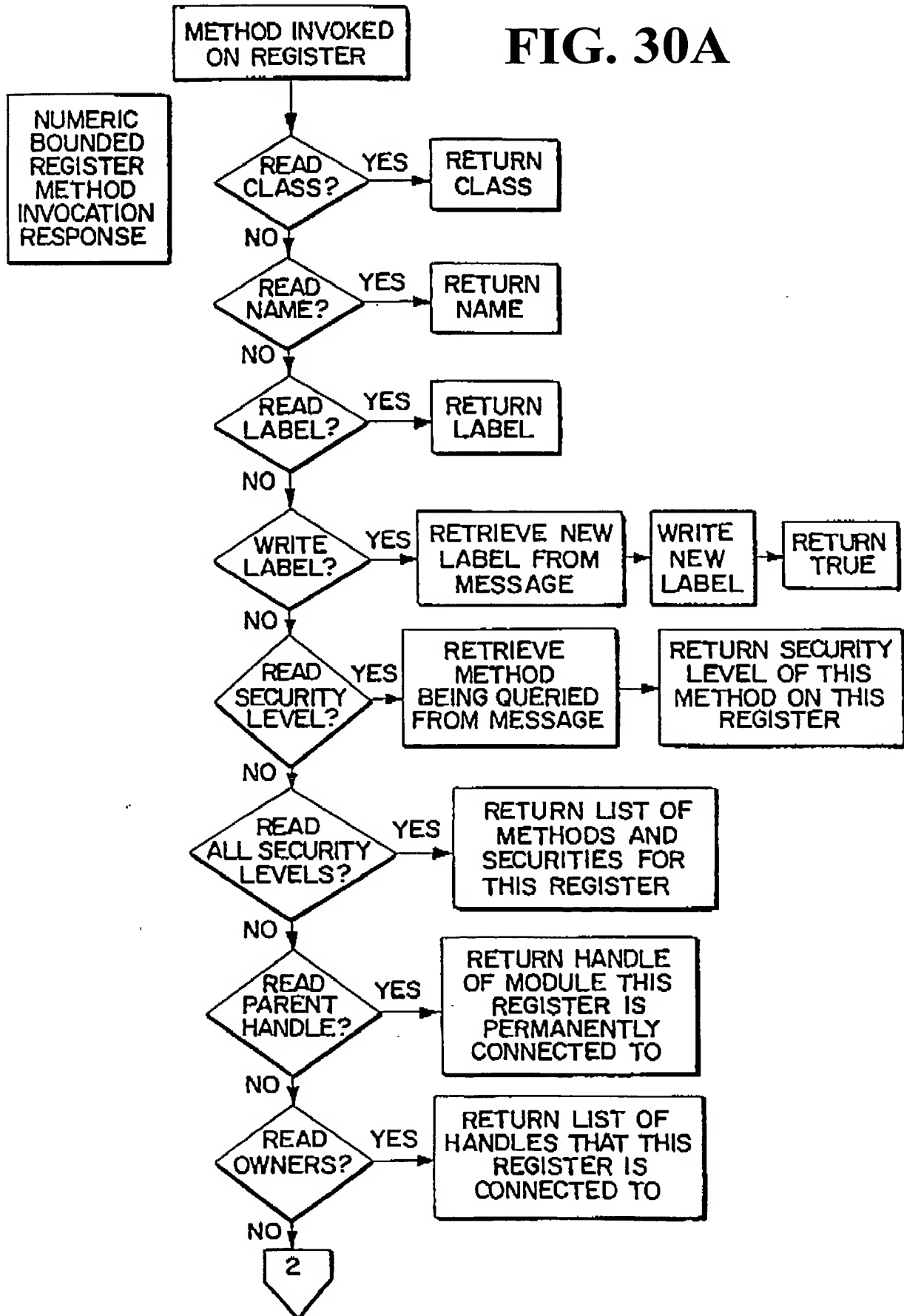
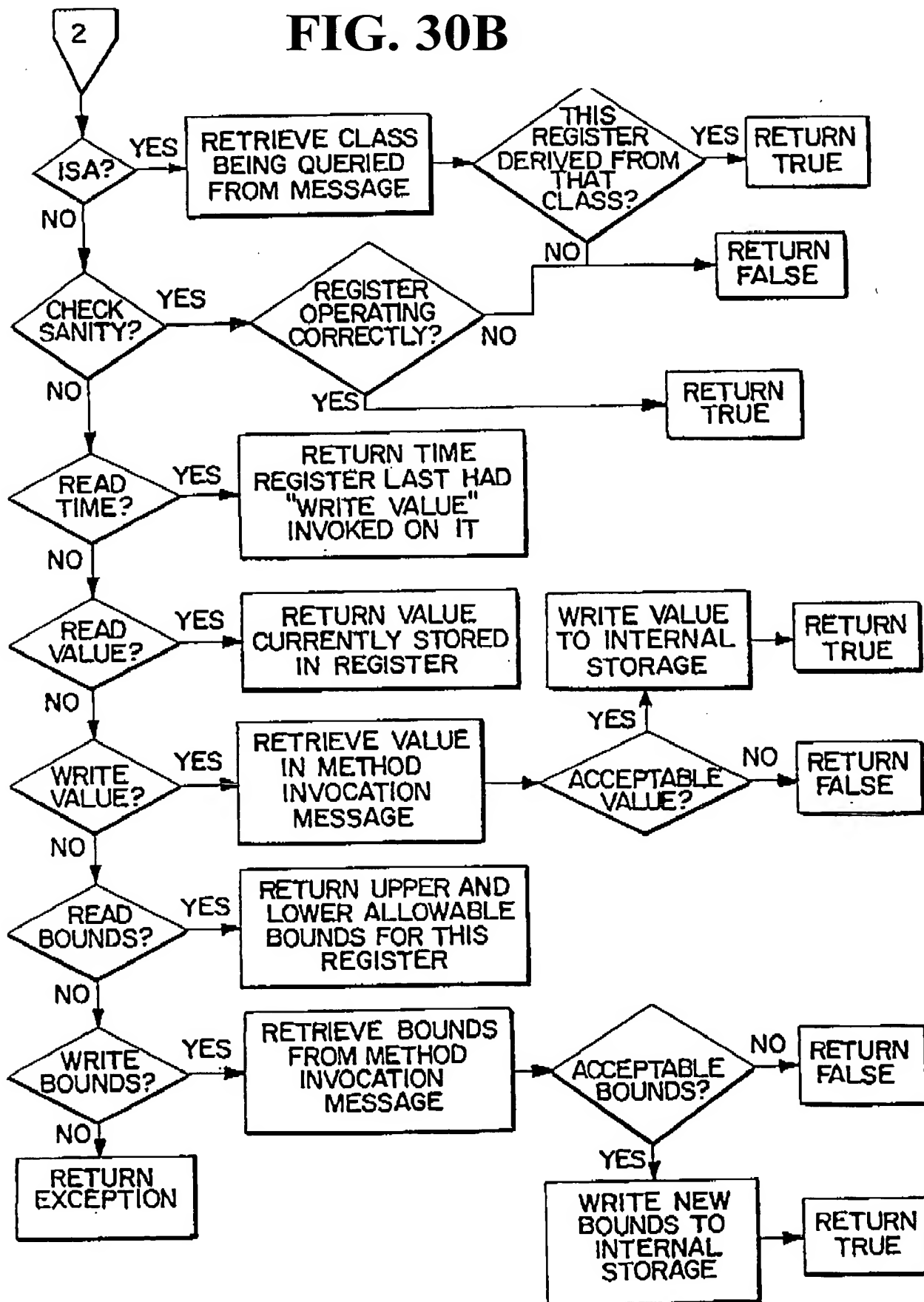
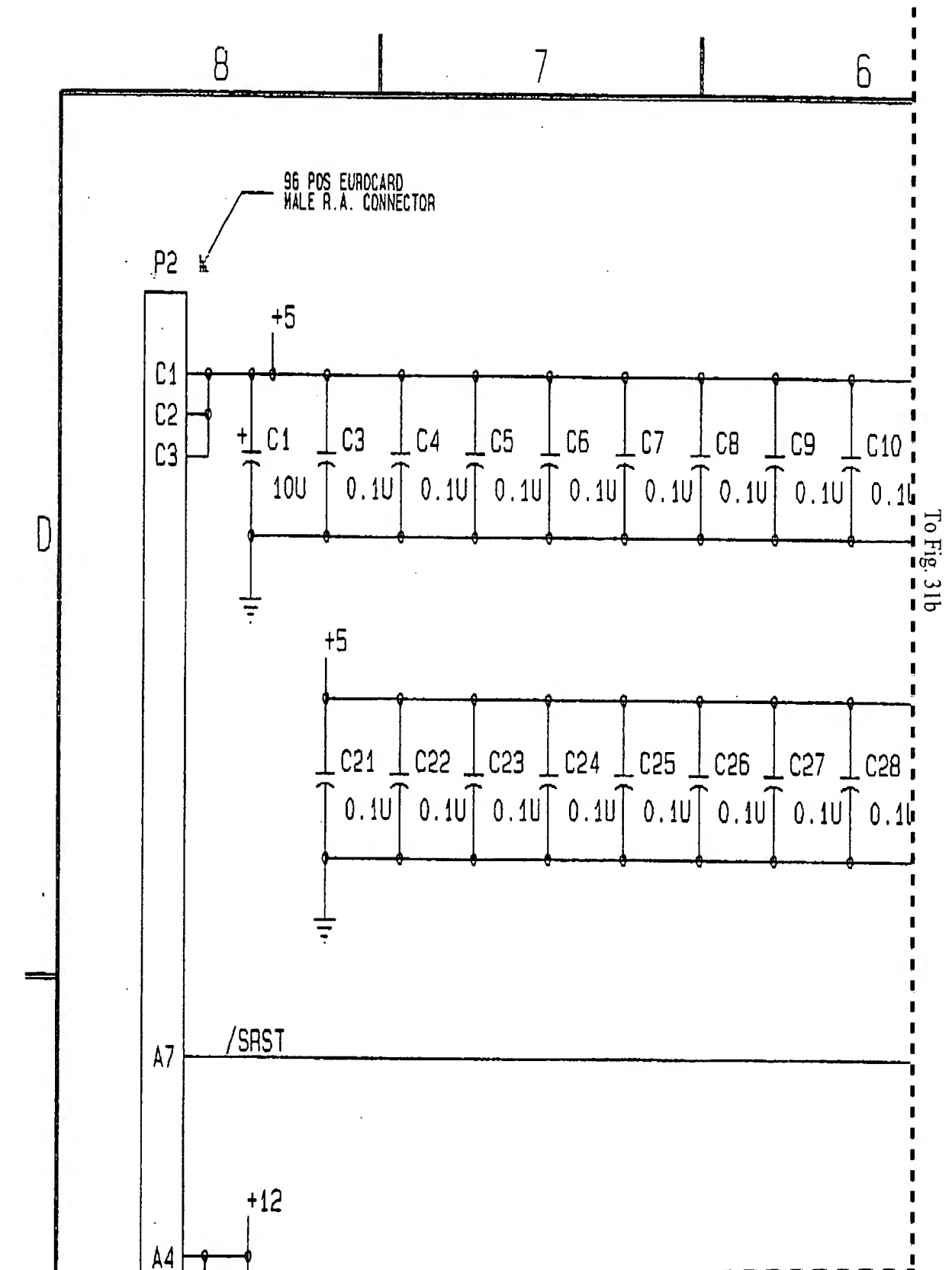


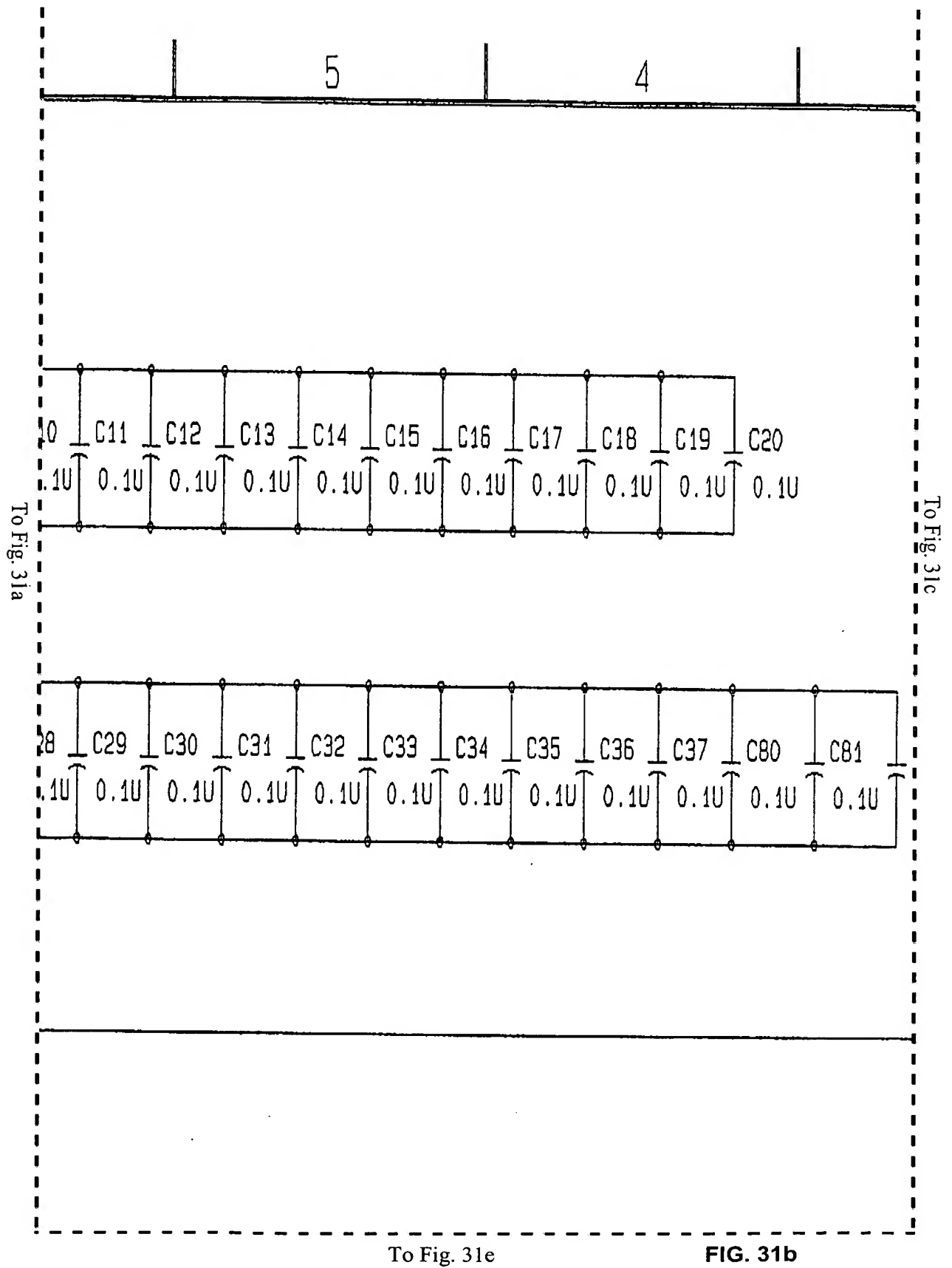
FIG. 30B

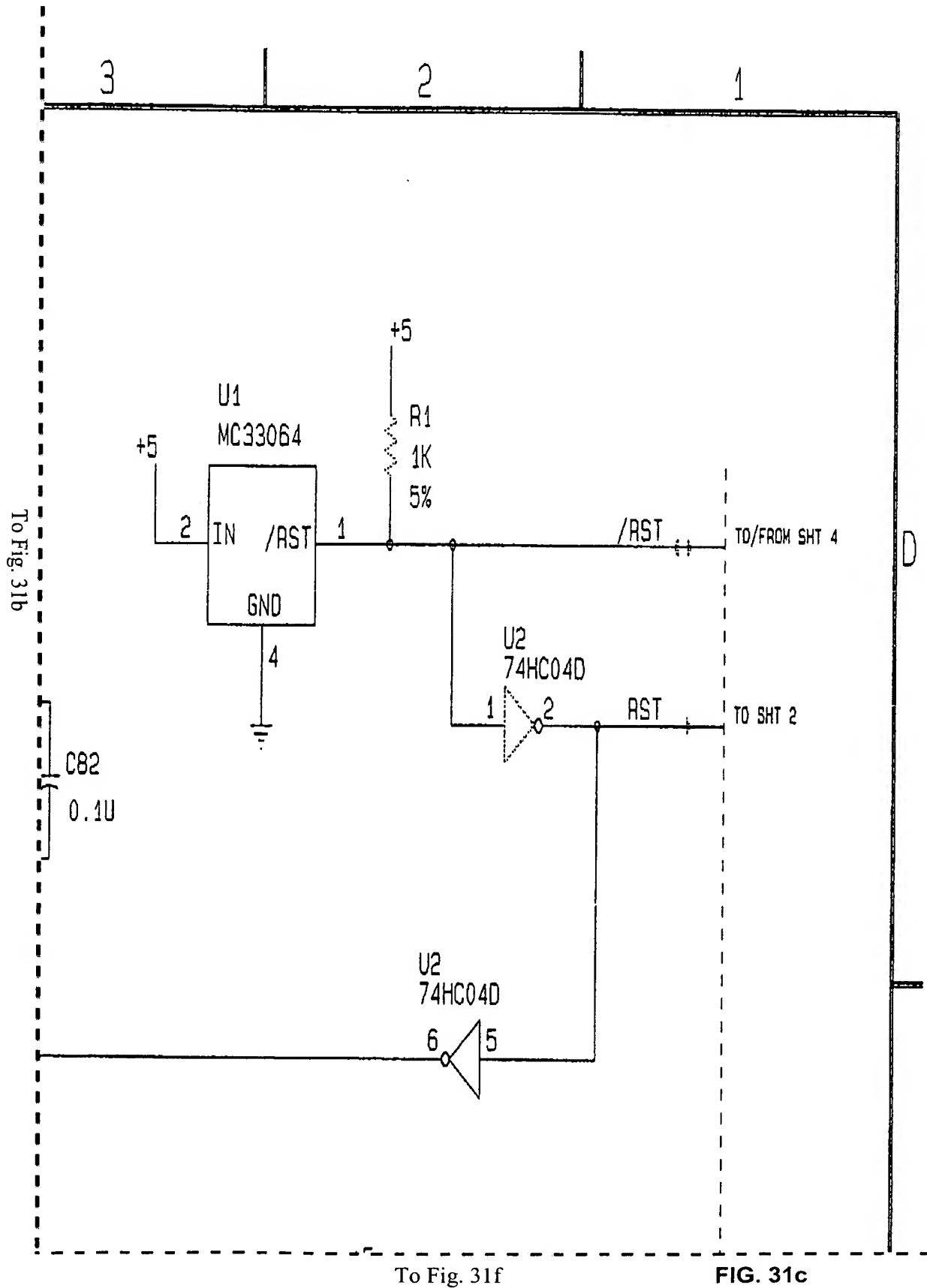




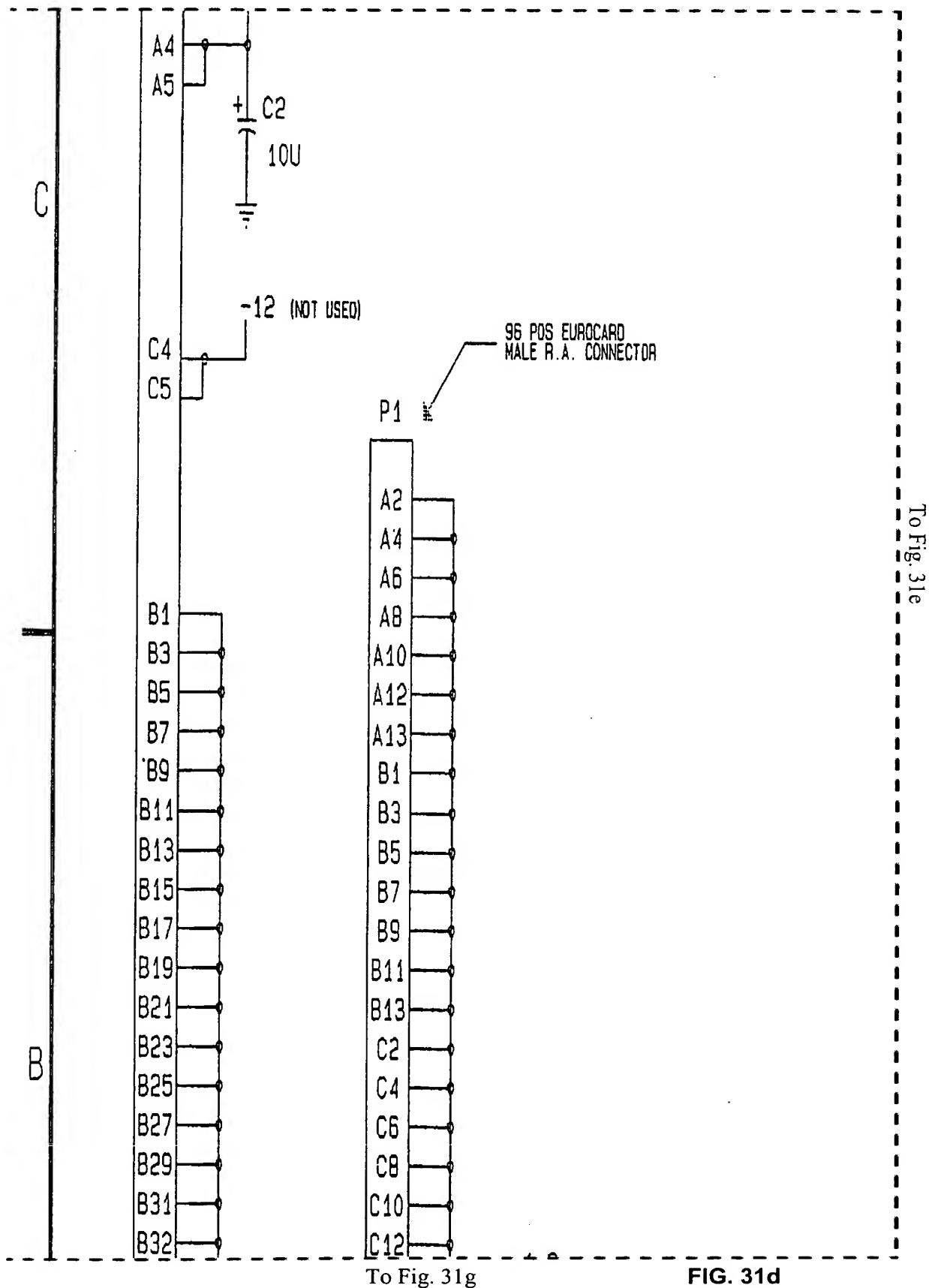
To Fig. 31d

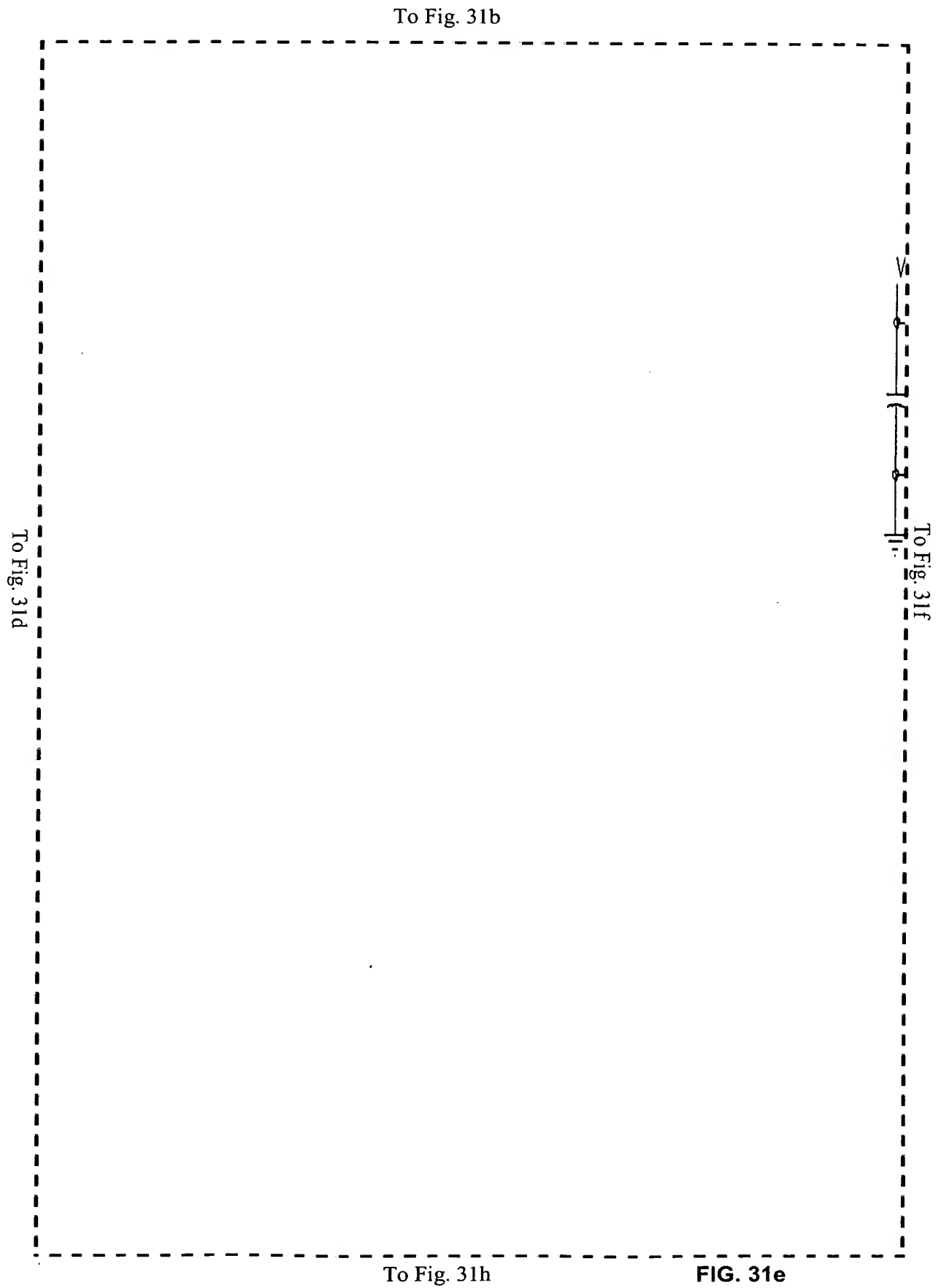
FIG. 31a



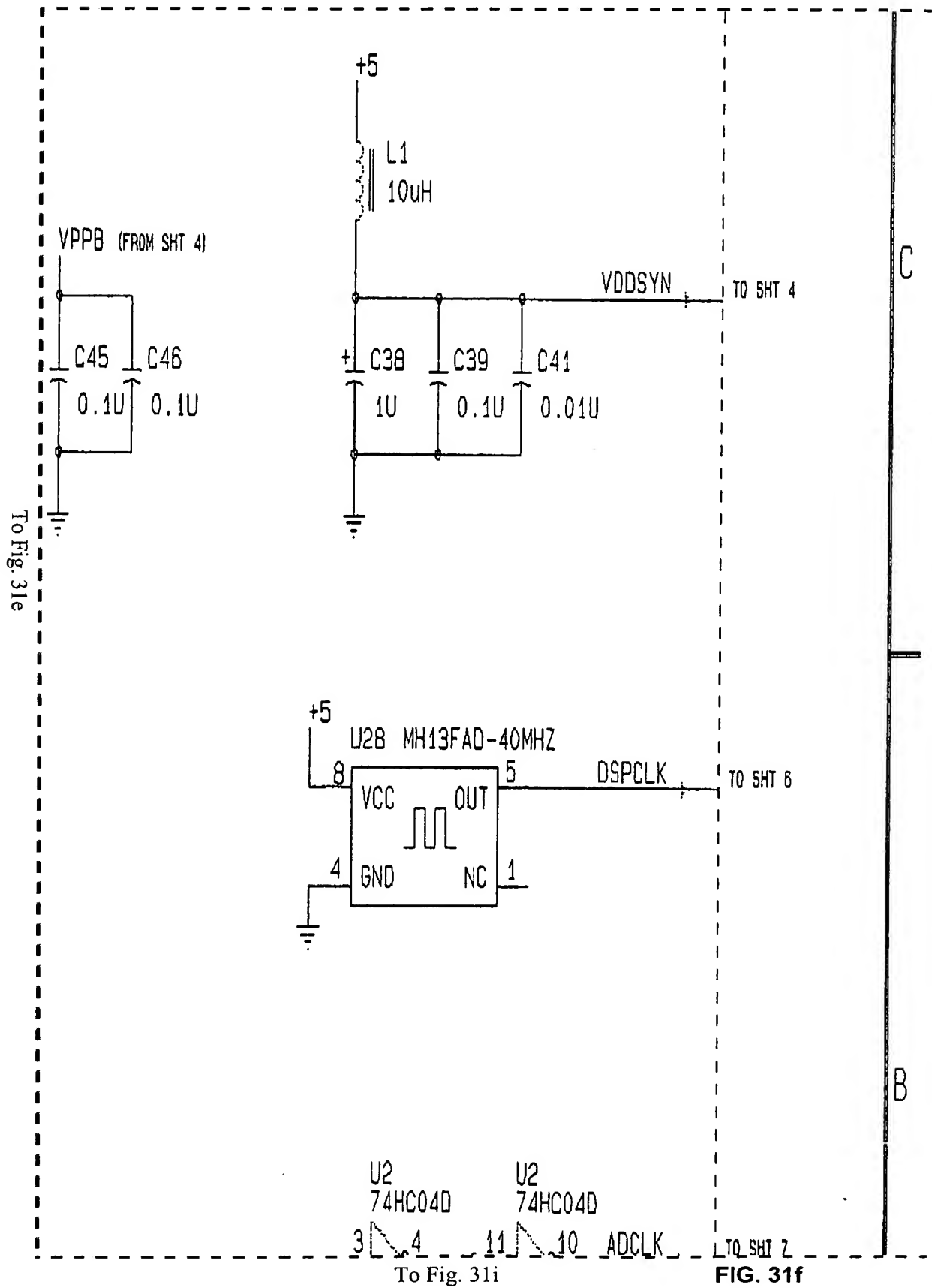


To Fig. 31a



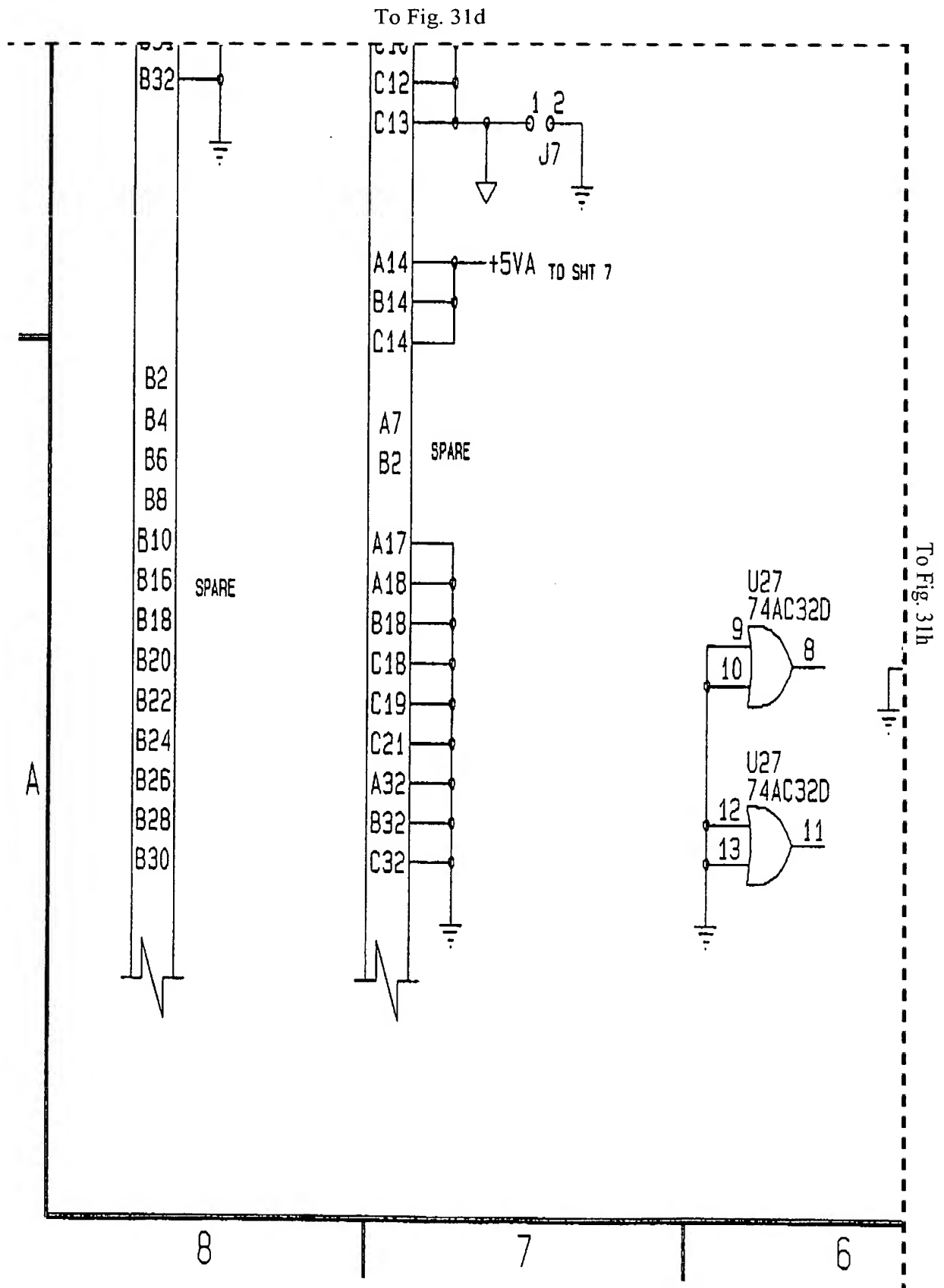


To Fig. 31c



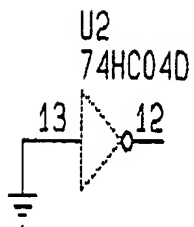
To Fig. 31i

FIG. 31f



To Fig. 31e

To Fig. 31g



To Fig. 31i

This schematic
proprietary
configuration
are issued in
or use shall
of CD Power M

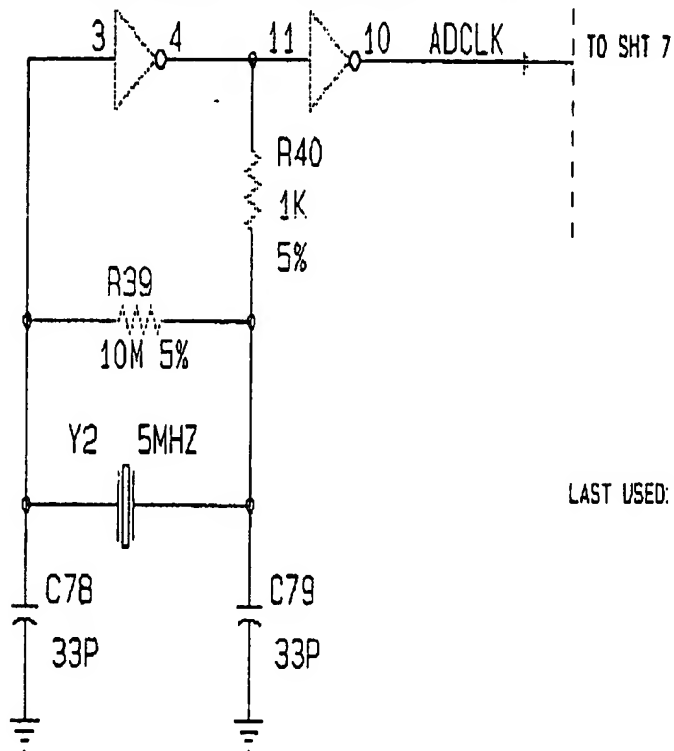
5

4

FIG. 31h

To Fig. 31f

To Fig. 31h



LAST USED: C83
R62
U28
P3
J17
TP11
DS2

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E

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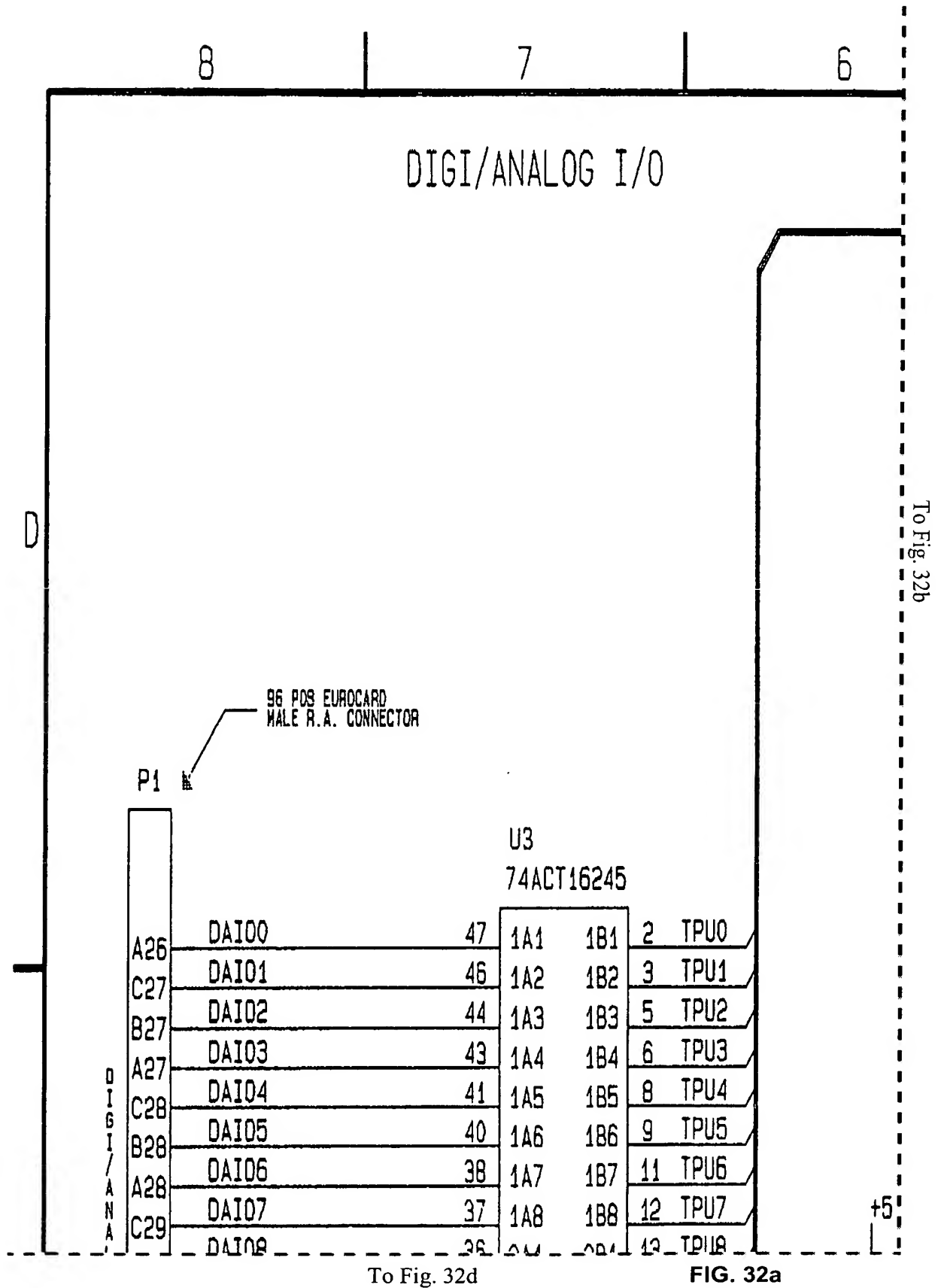
SHEET 1 OF 7

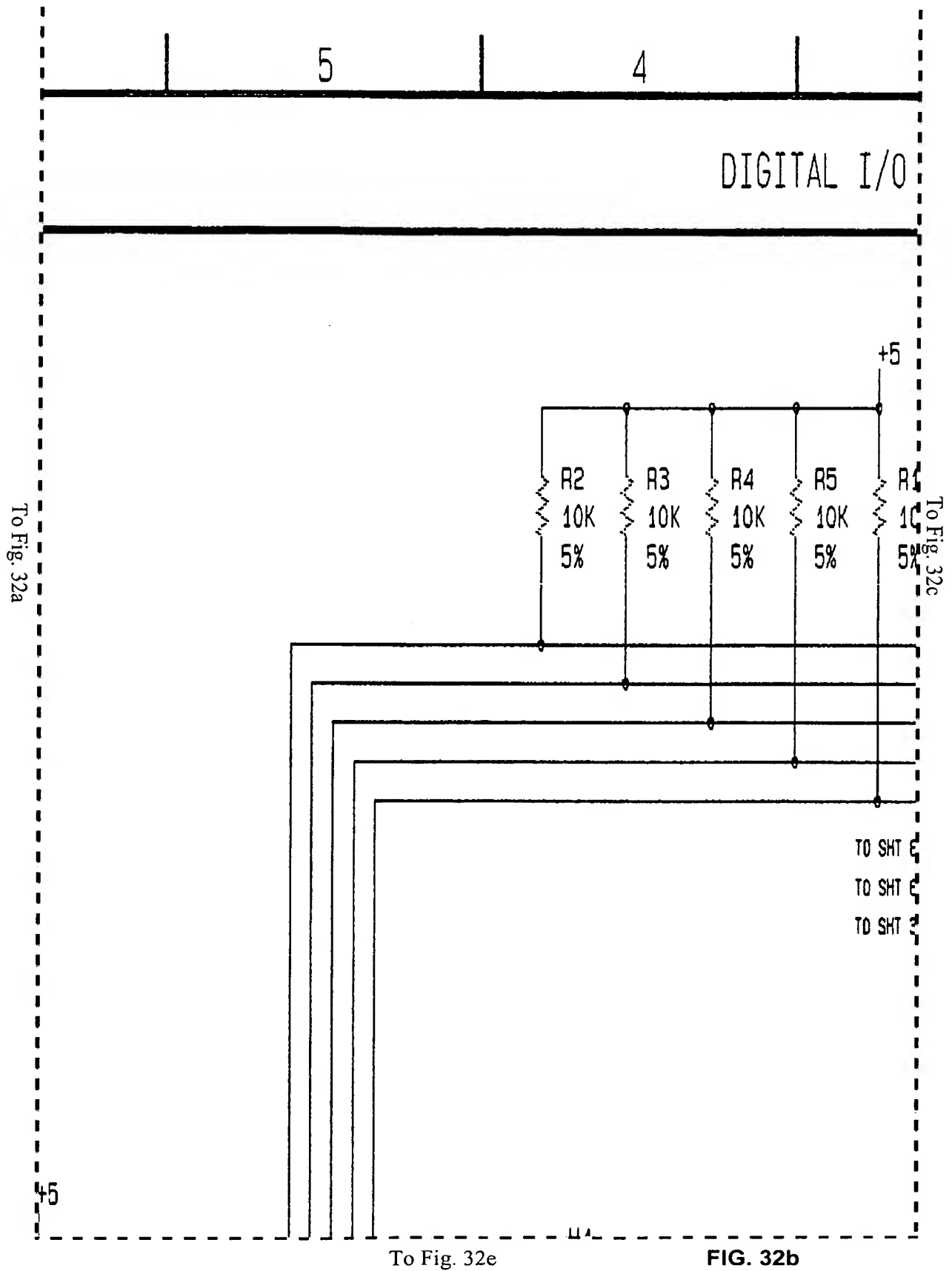
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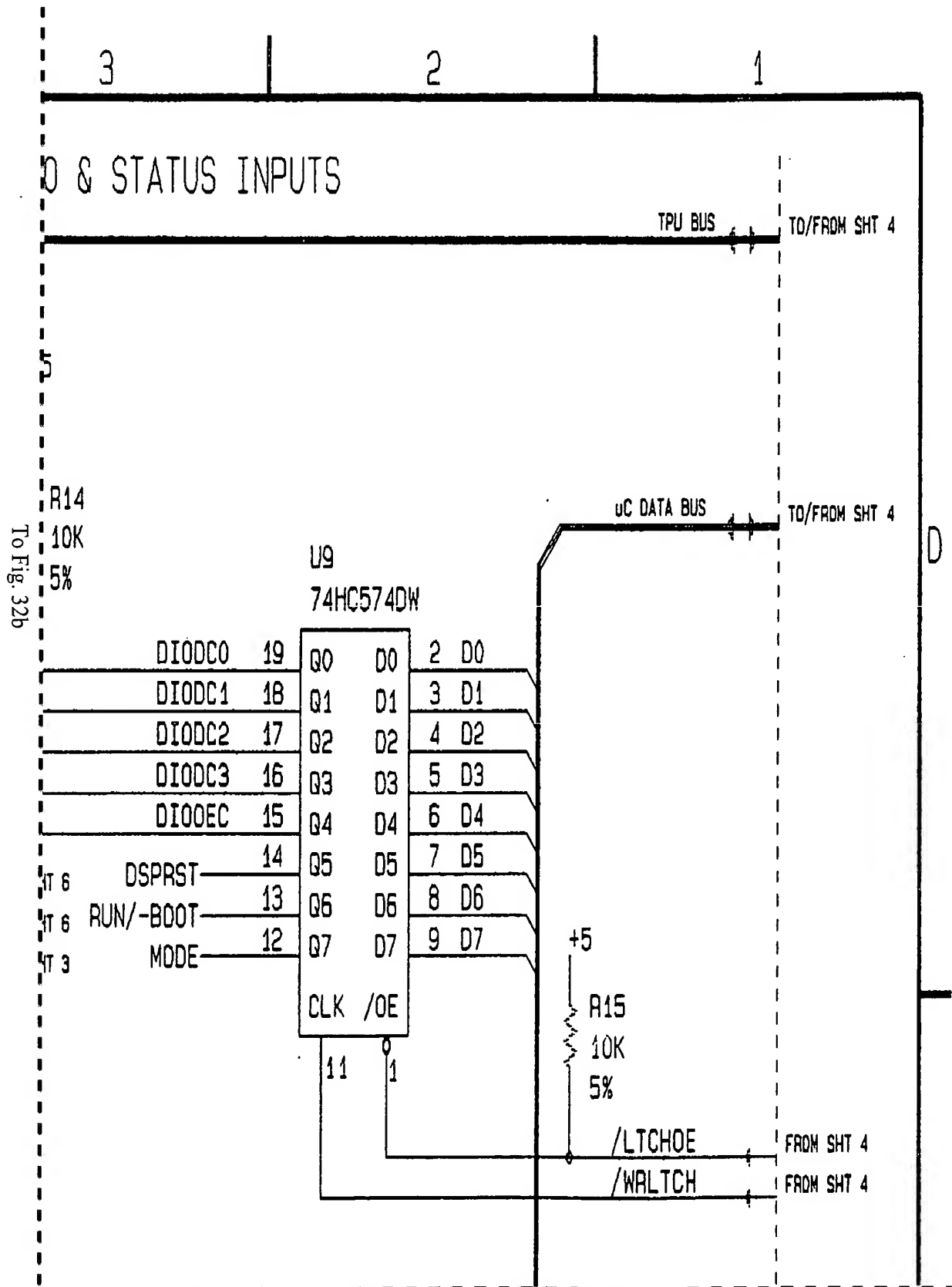
2

1

FIG. 31i





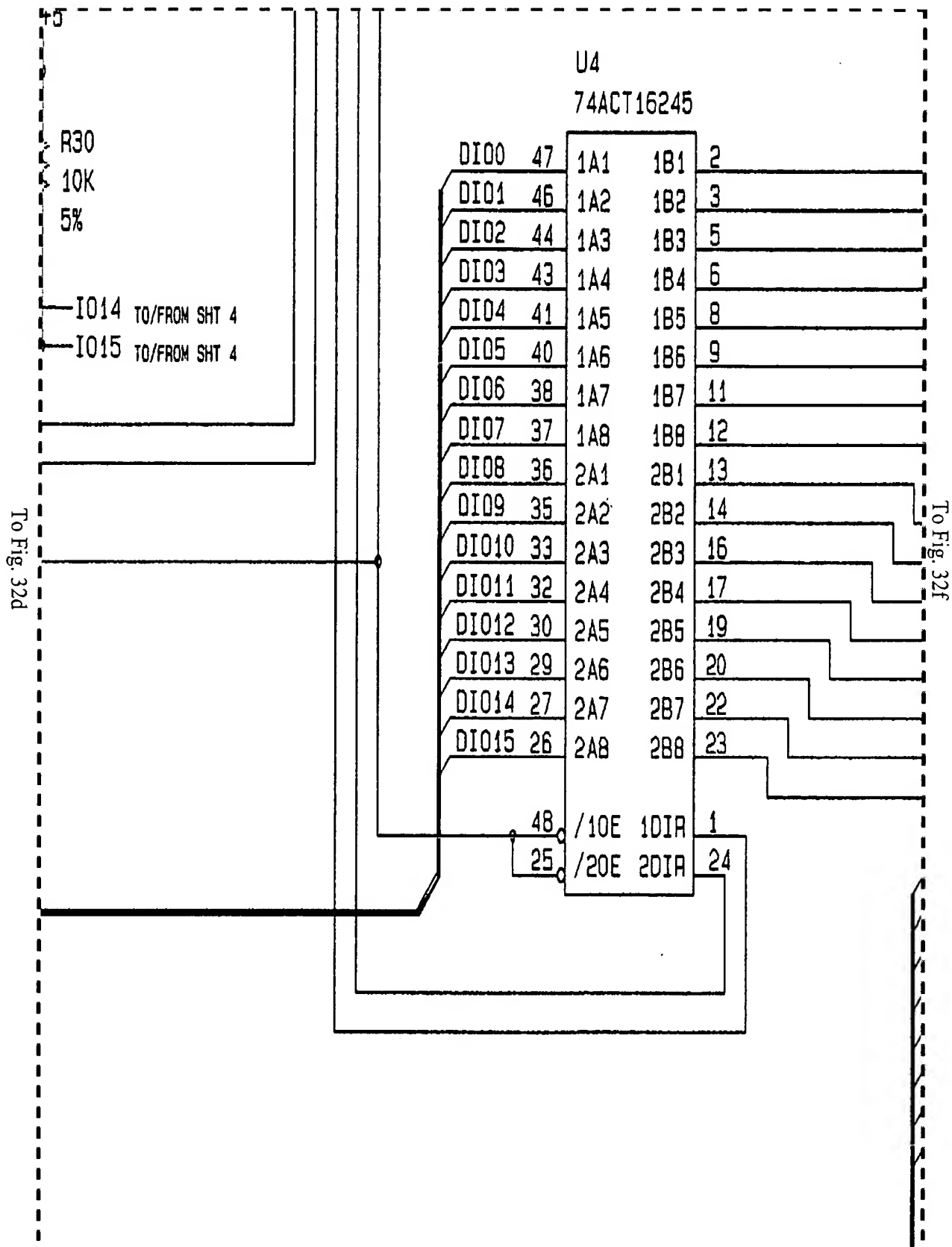


To Fig. 32f

FIG. 32c

FIG. 32d

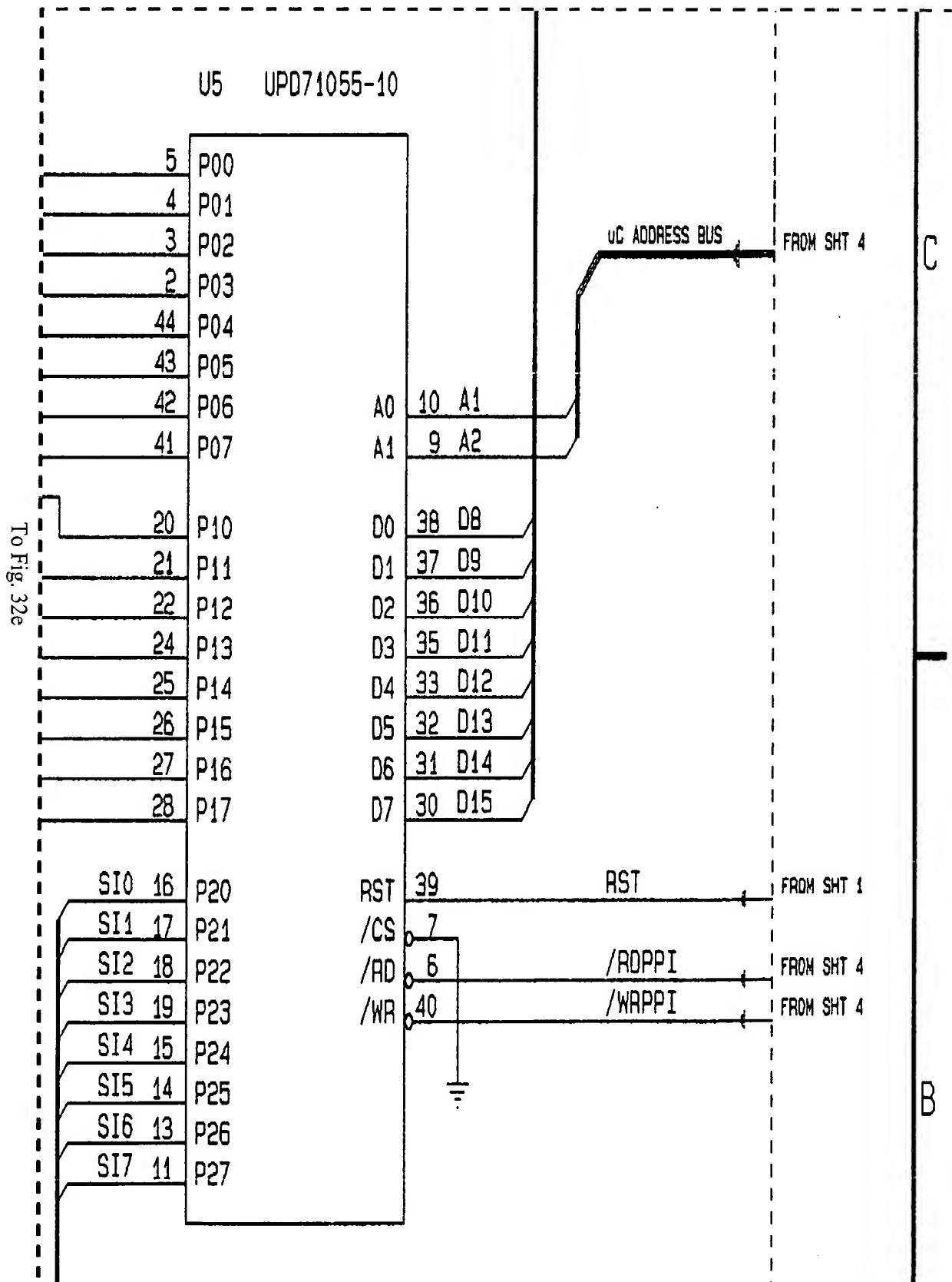
To Fig. 32b



To Fig. 32h

FIG. 32e

To Fig. 32c



To Fig. 32i

FIG. 32f

To Fig. 32d

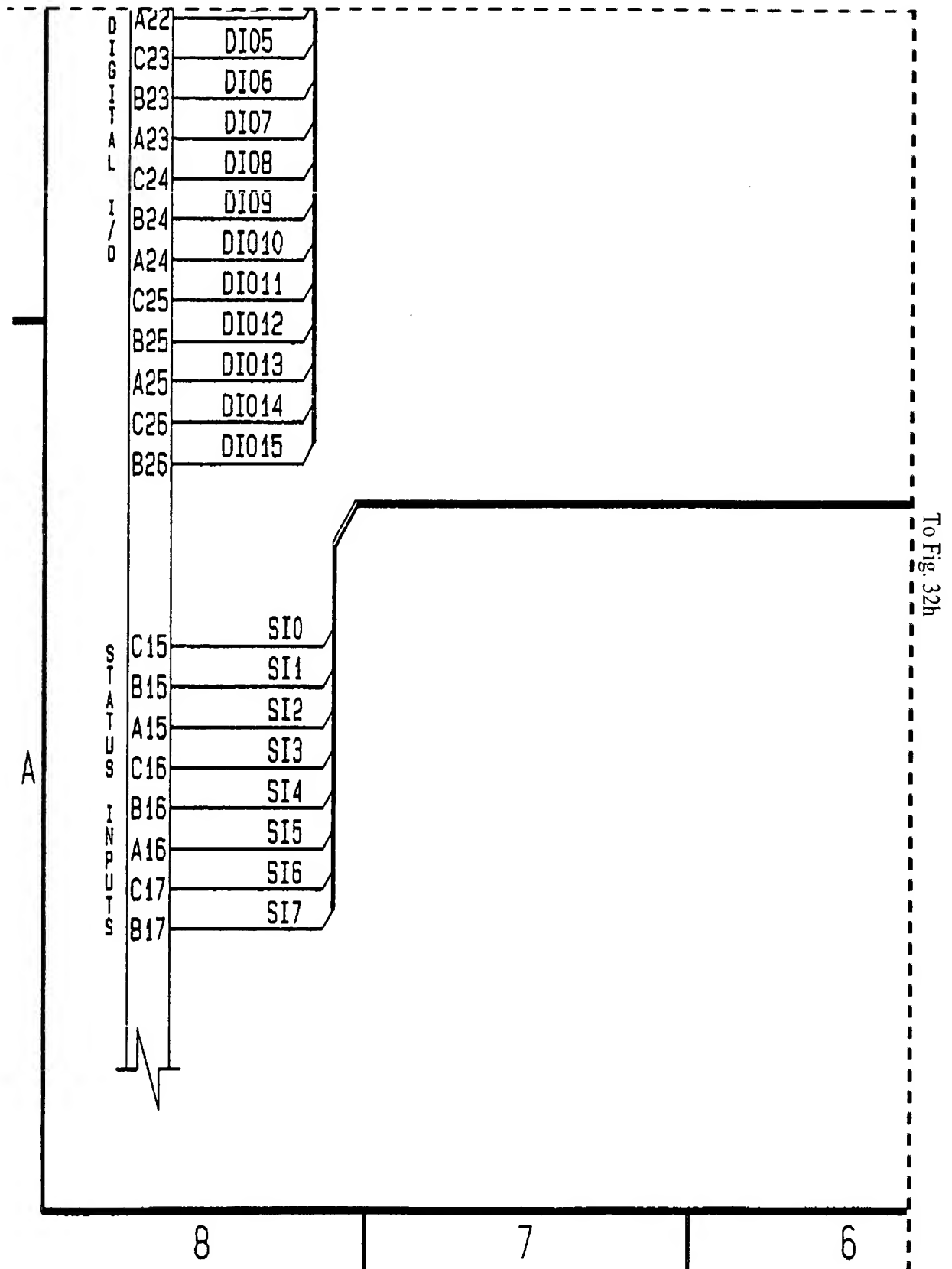


FIG. 32g

To Fig. 32e

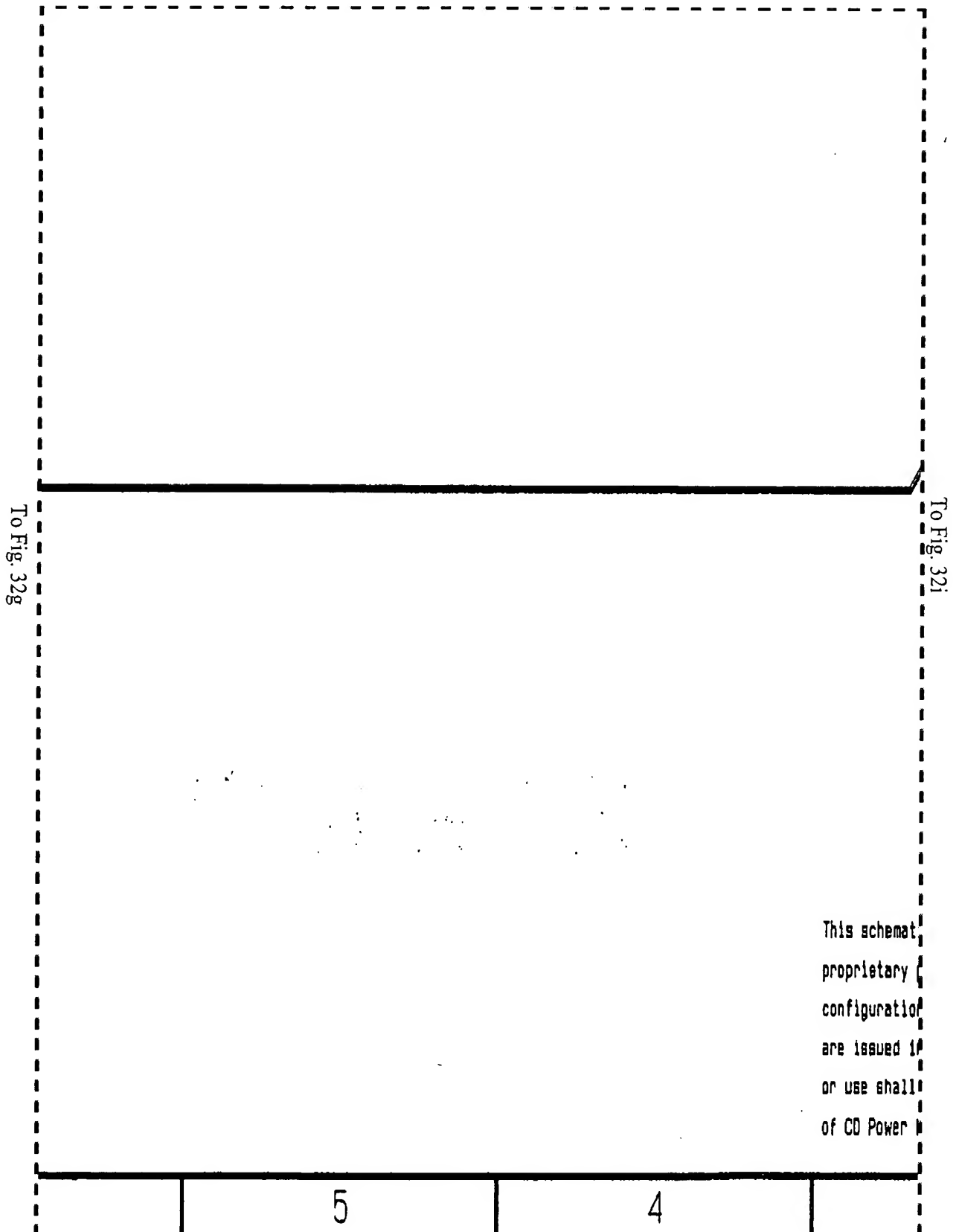
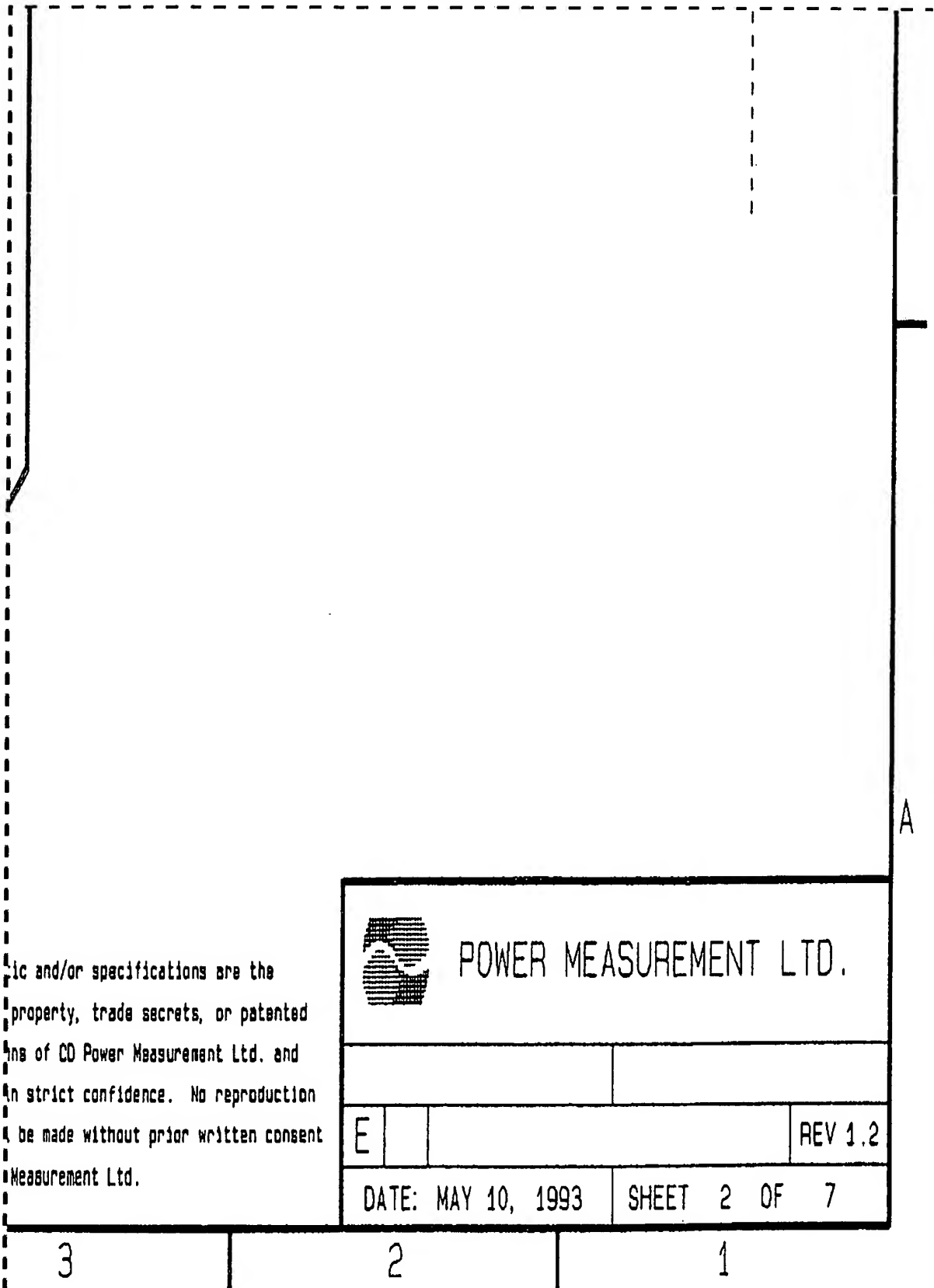


FIG. 32h

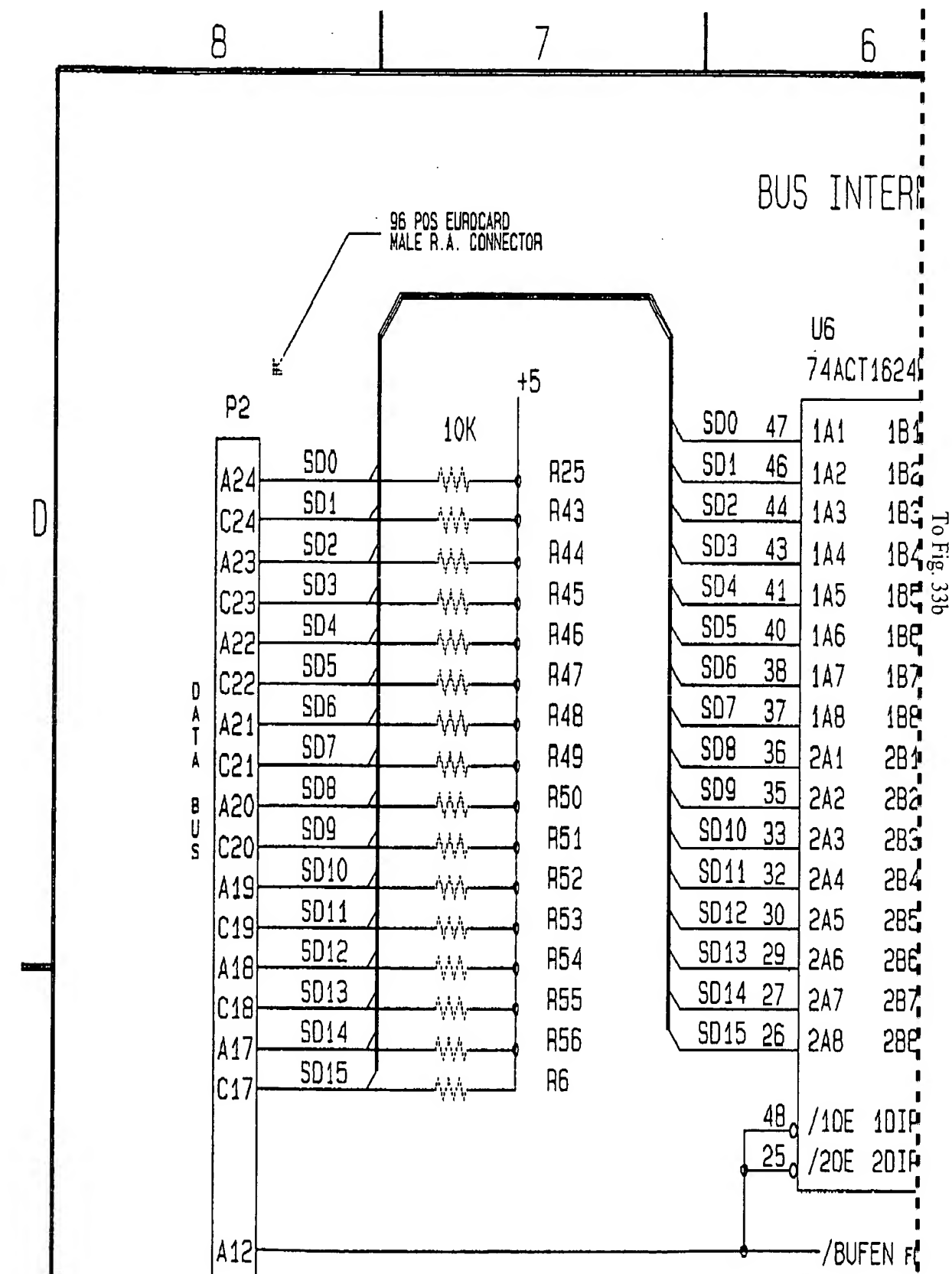
To Fig. 32f

To Fig. 32h



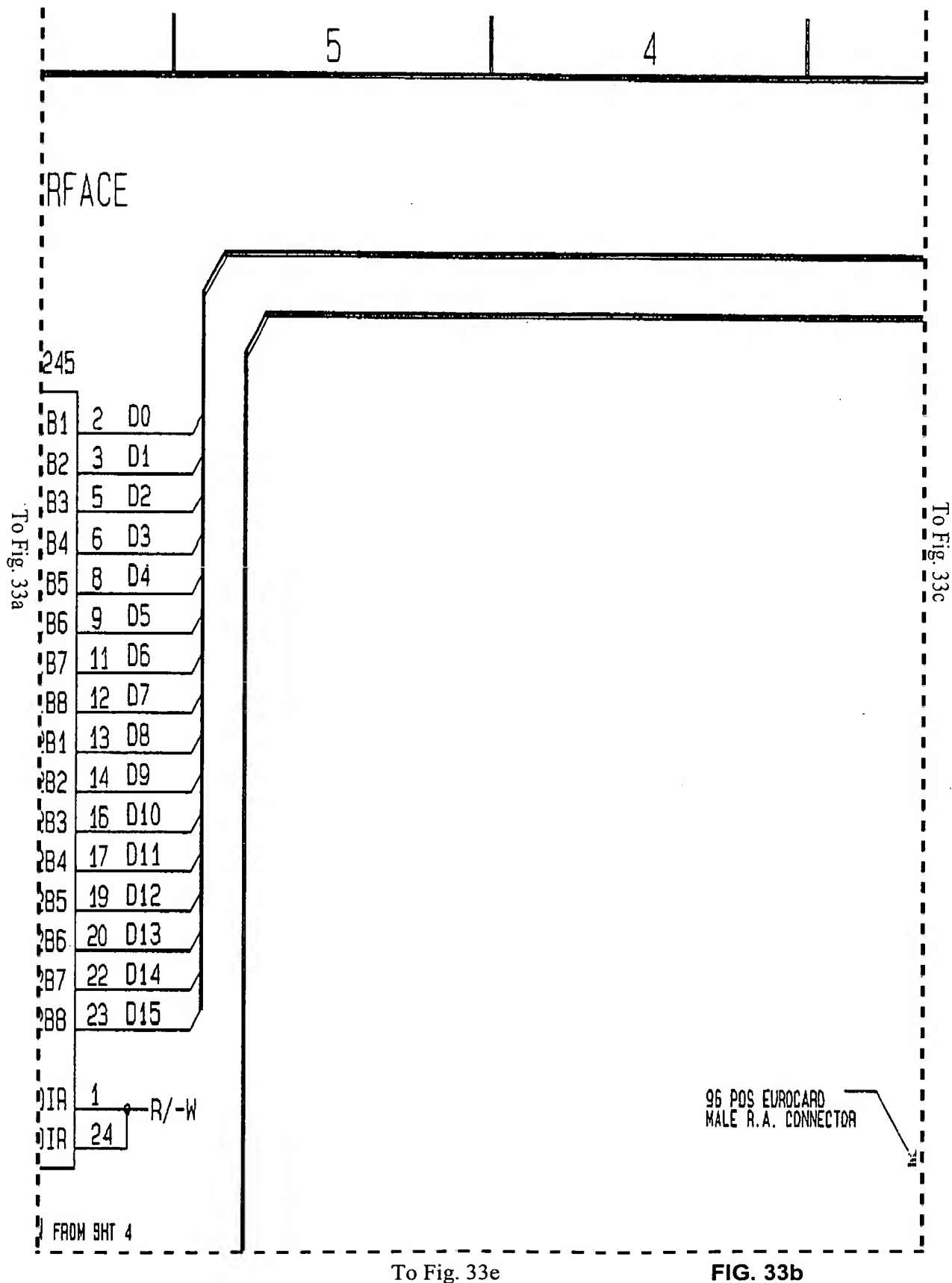
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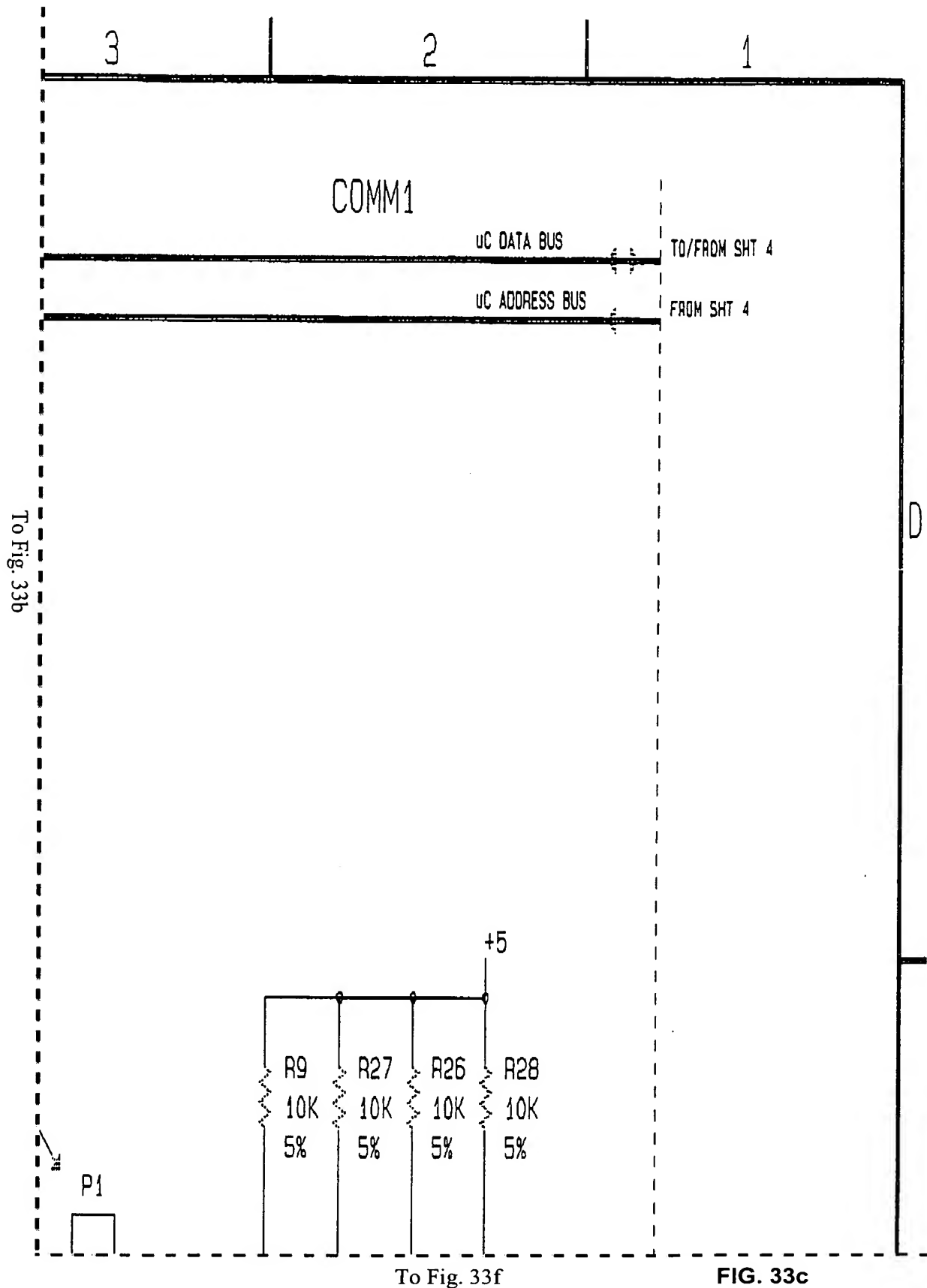
FIG. 32i



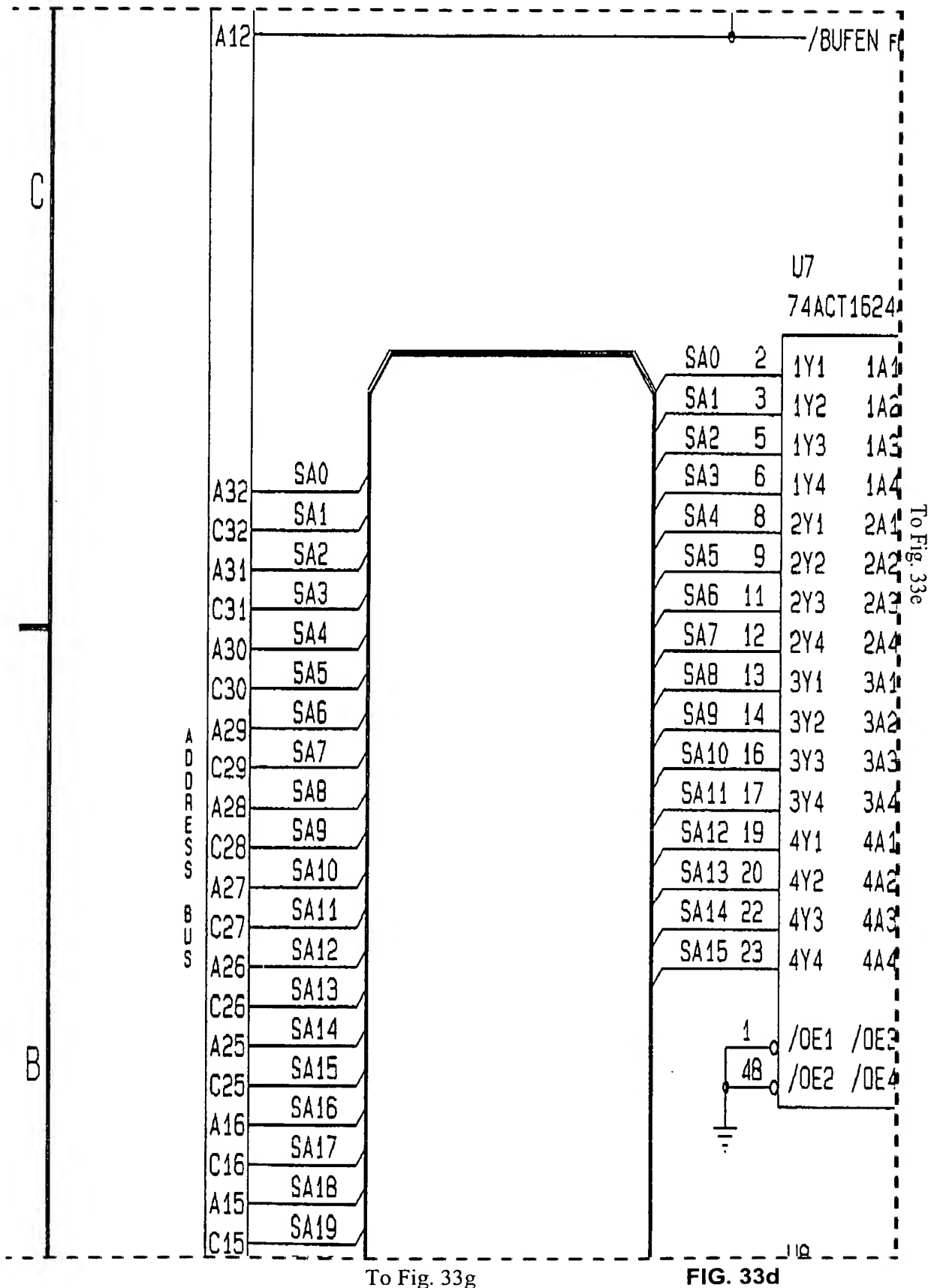
To Fig. 33d

FIG. 33a



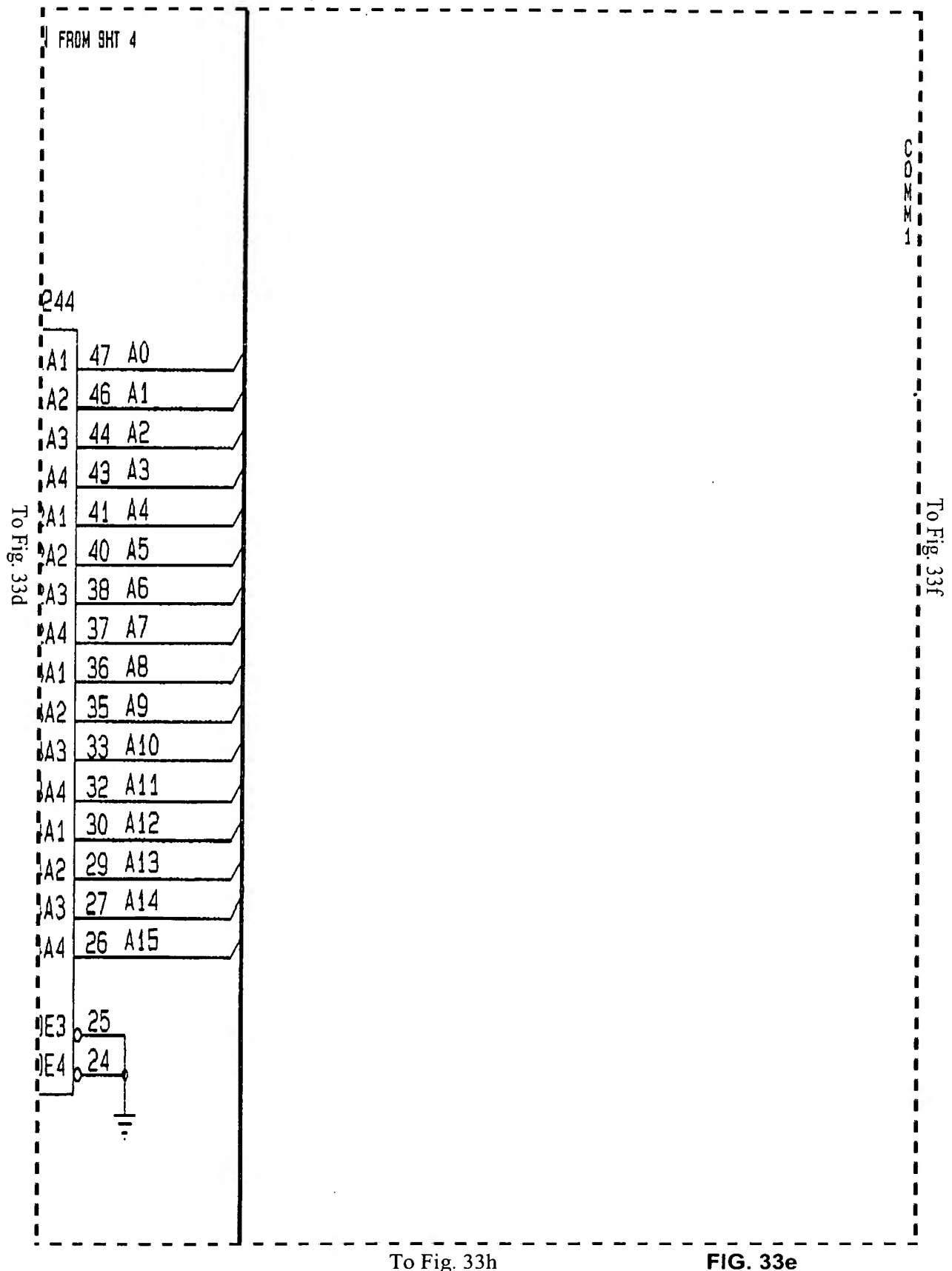


To Fig. 33a

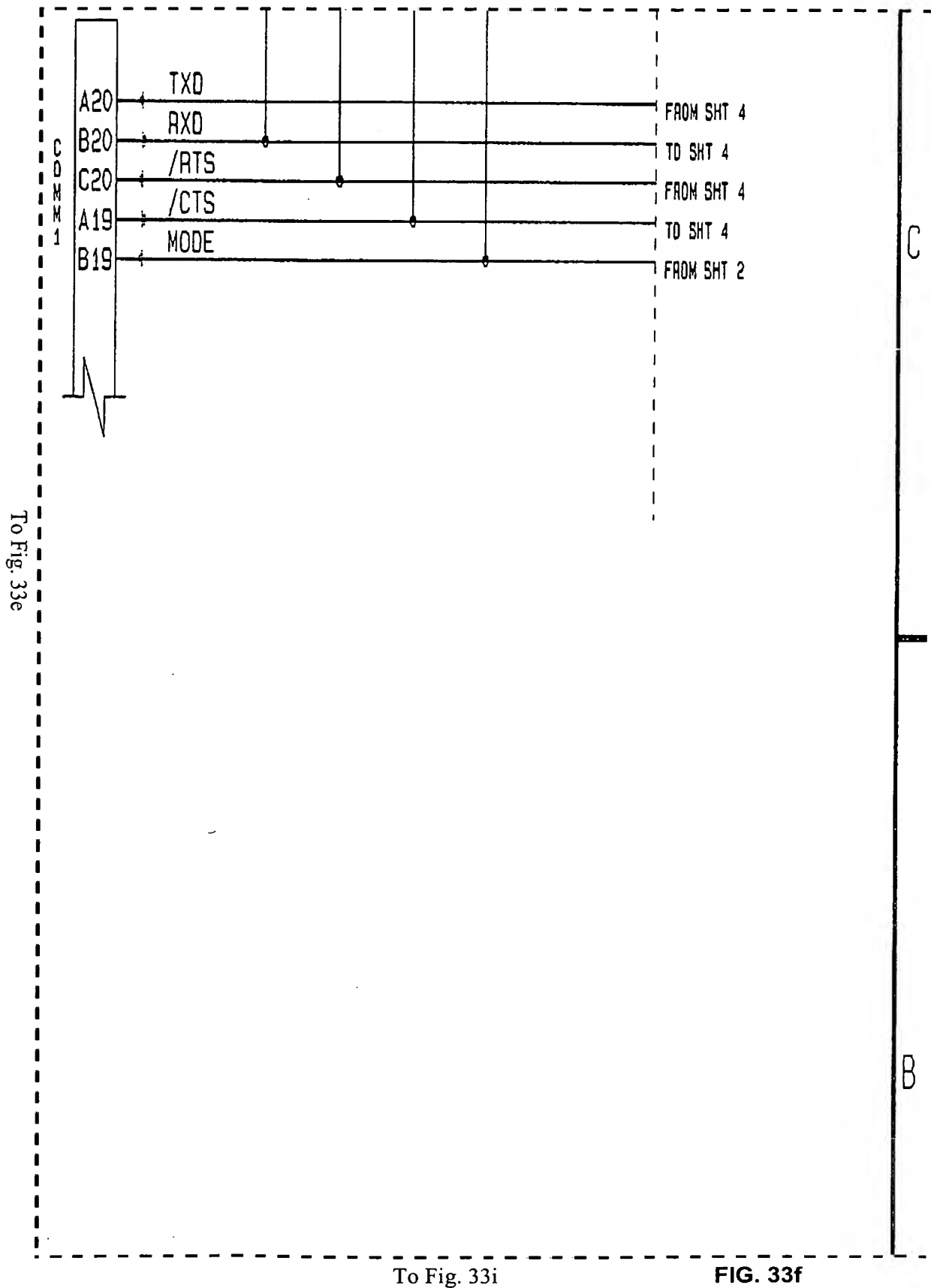


To Fig. 33g

To Fig. 33b



To Fig. 33c



To Fig. 33d

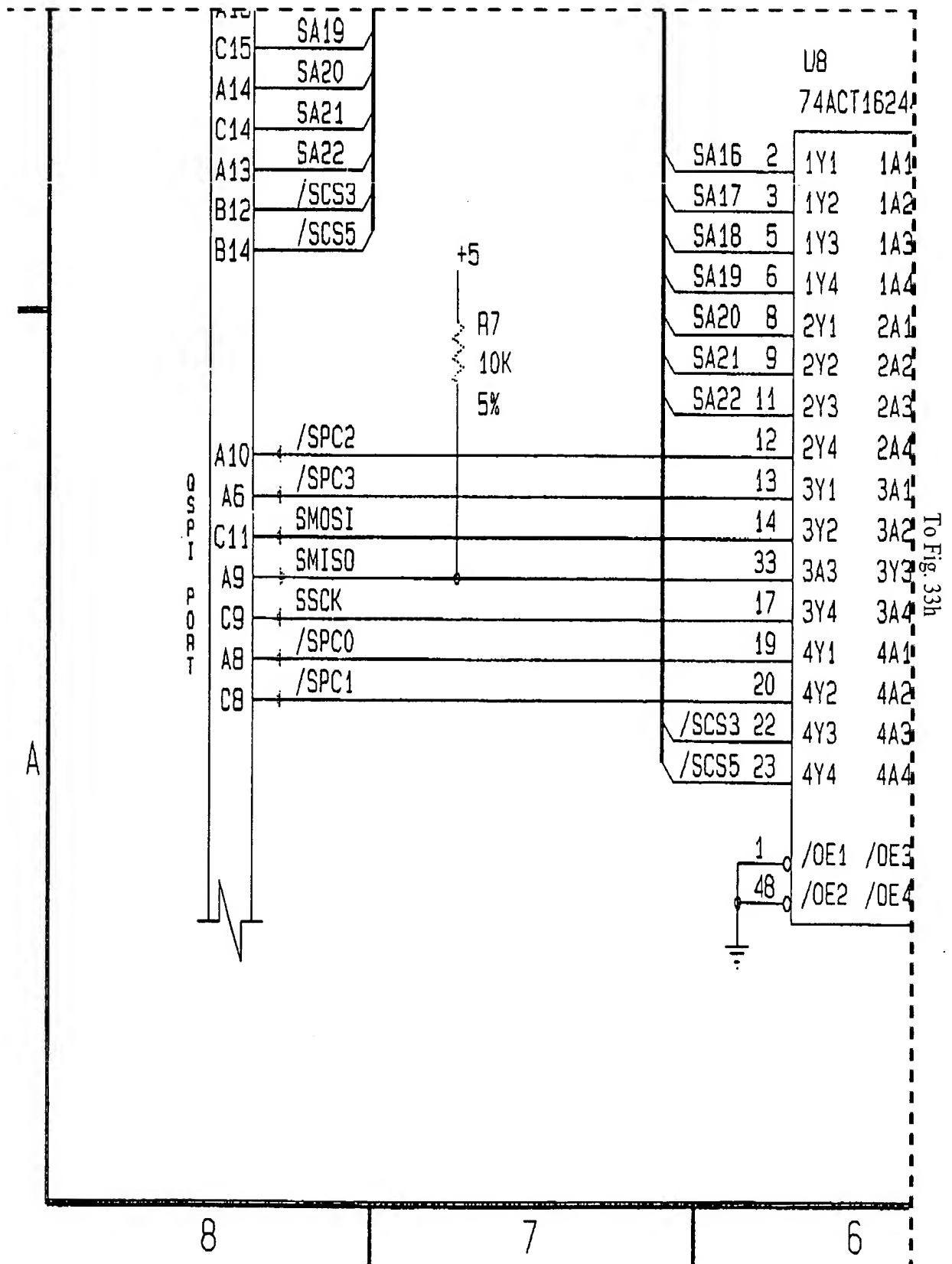


FIG. 33g

To Fig. 33e

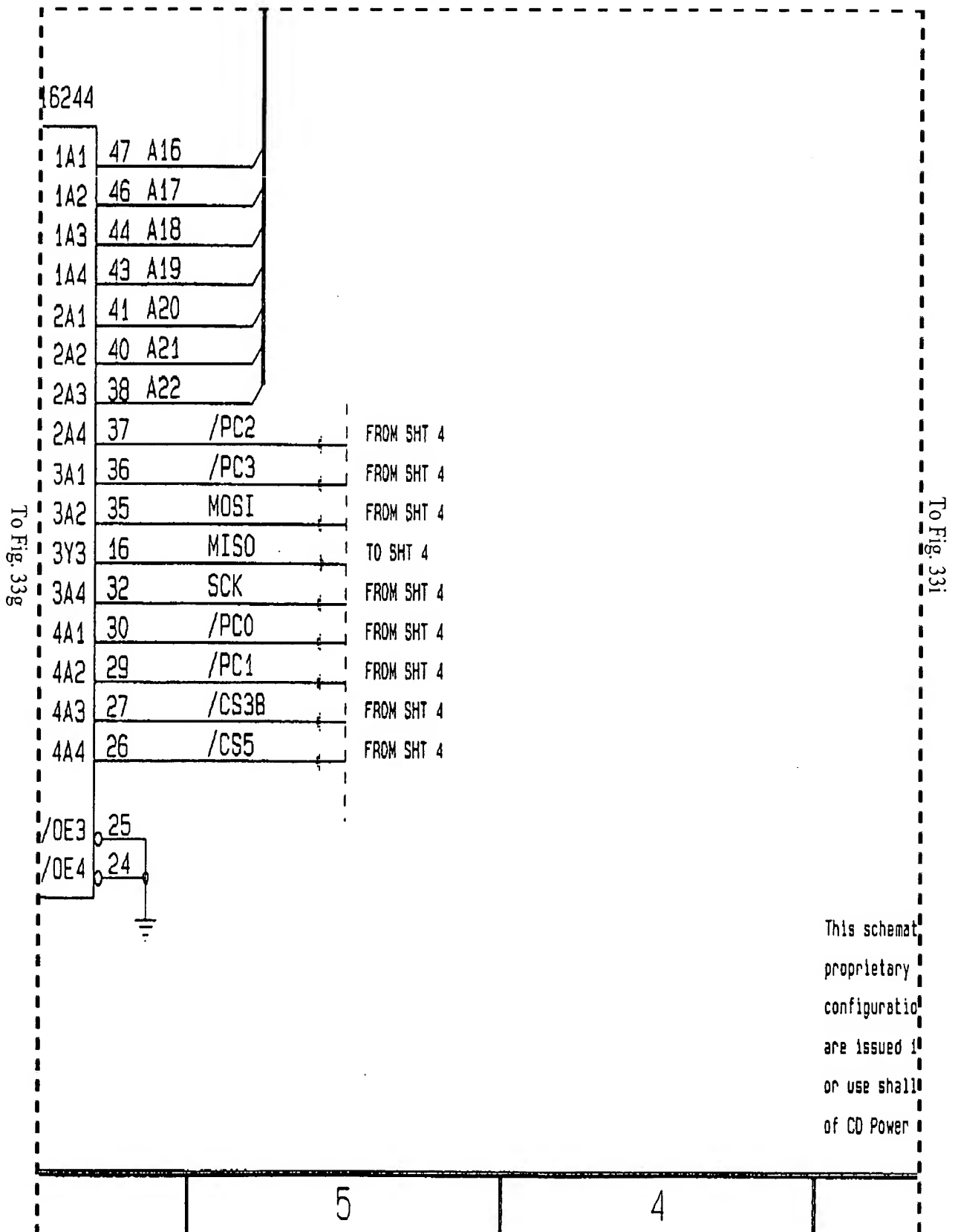


FIG. 33h

To Fig. 33f

To Fig. 33h

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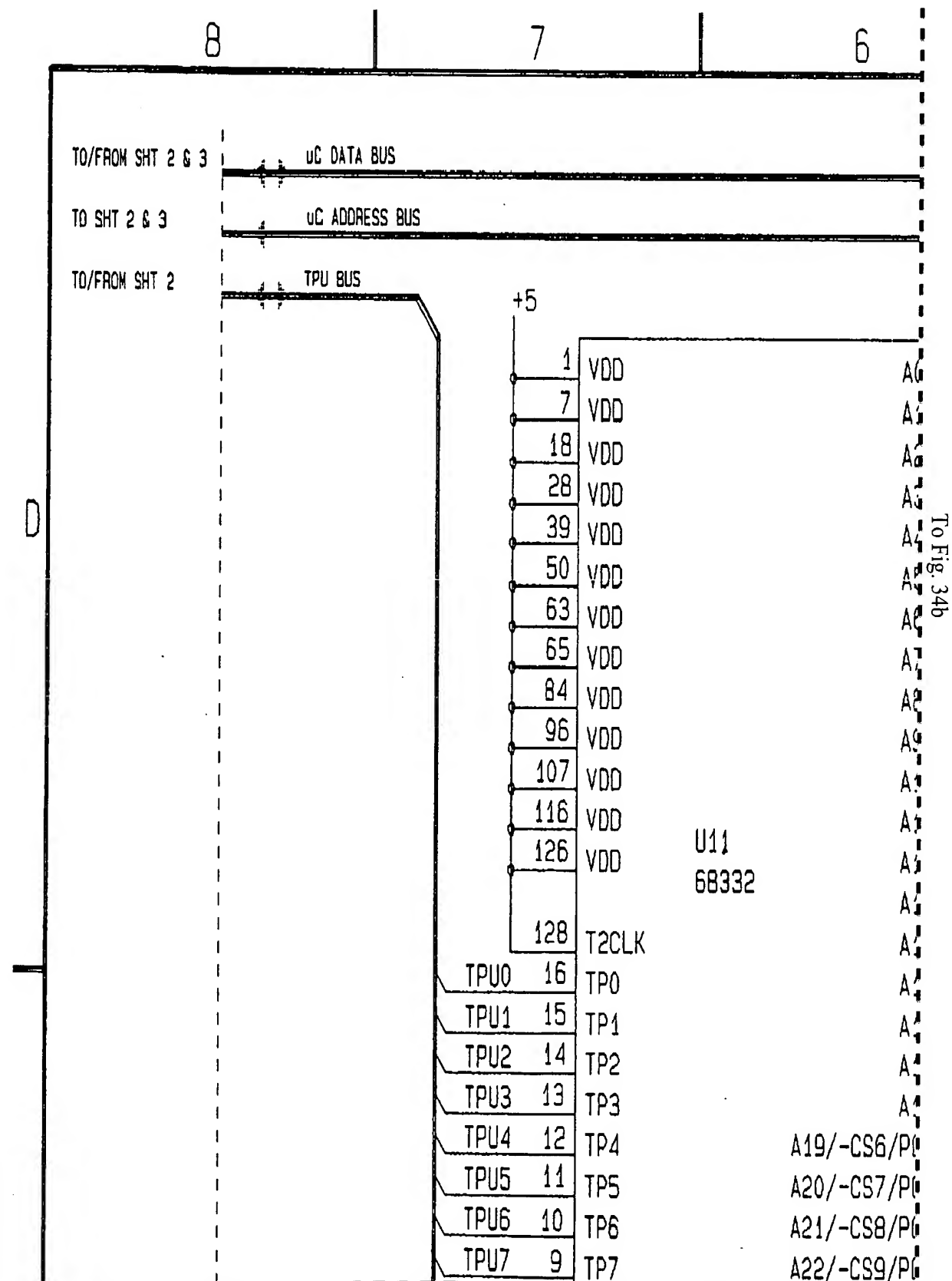
SHEET 3 OF 7

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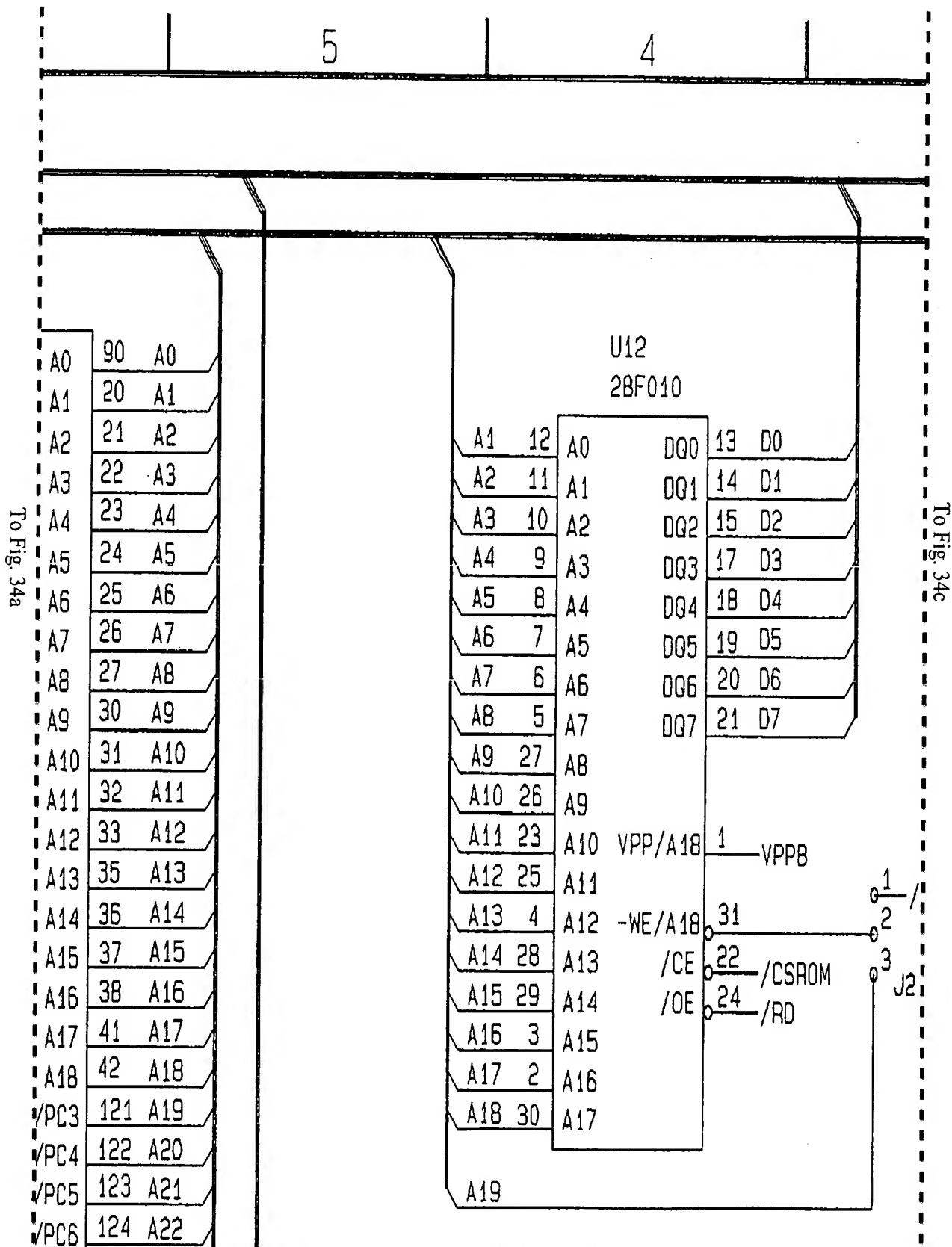
1

FIG. 33i



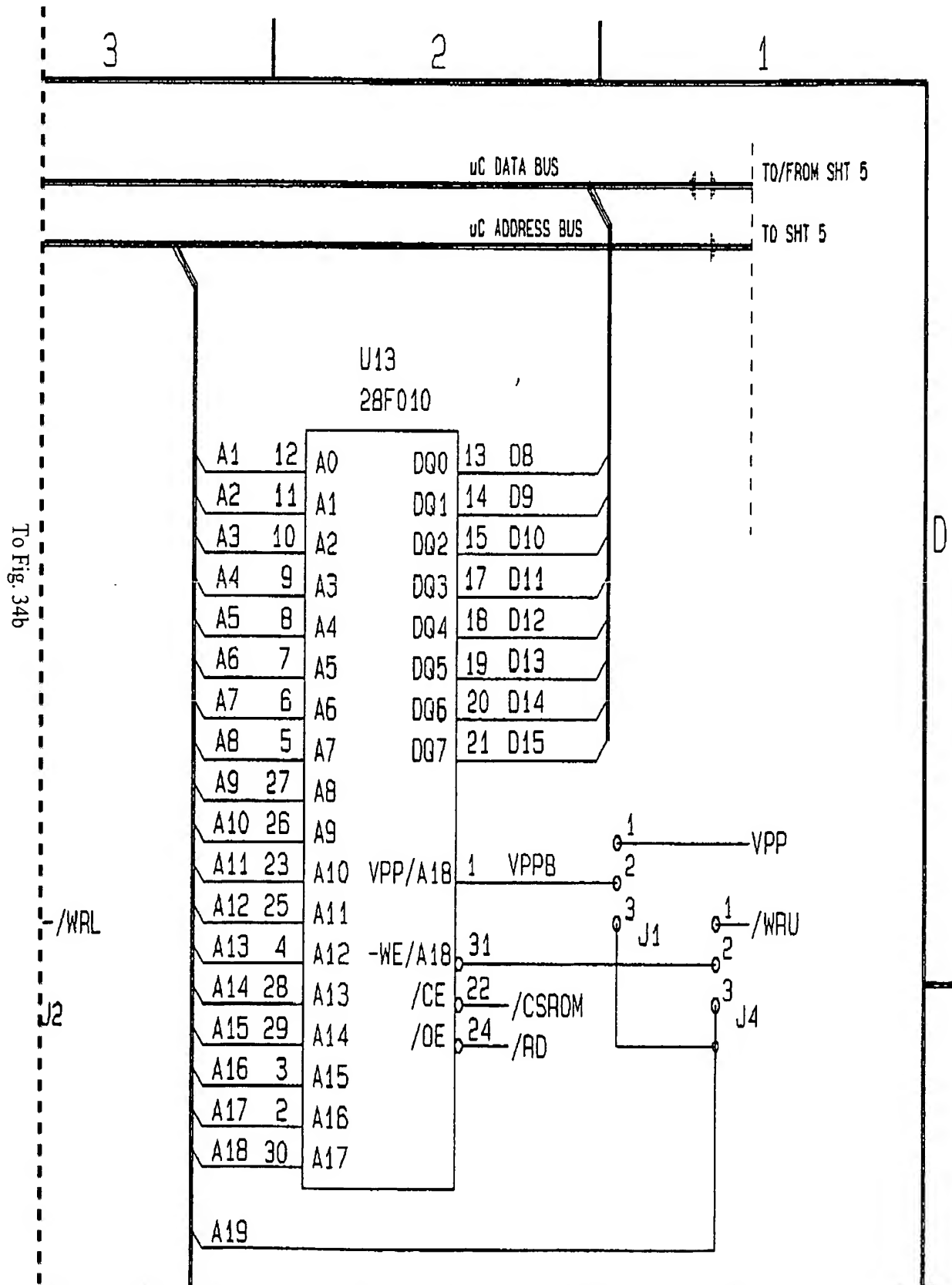
To Fig. 34d

FIG. 34a



To Fig. 34e

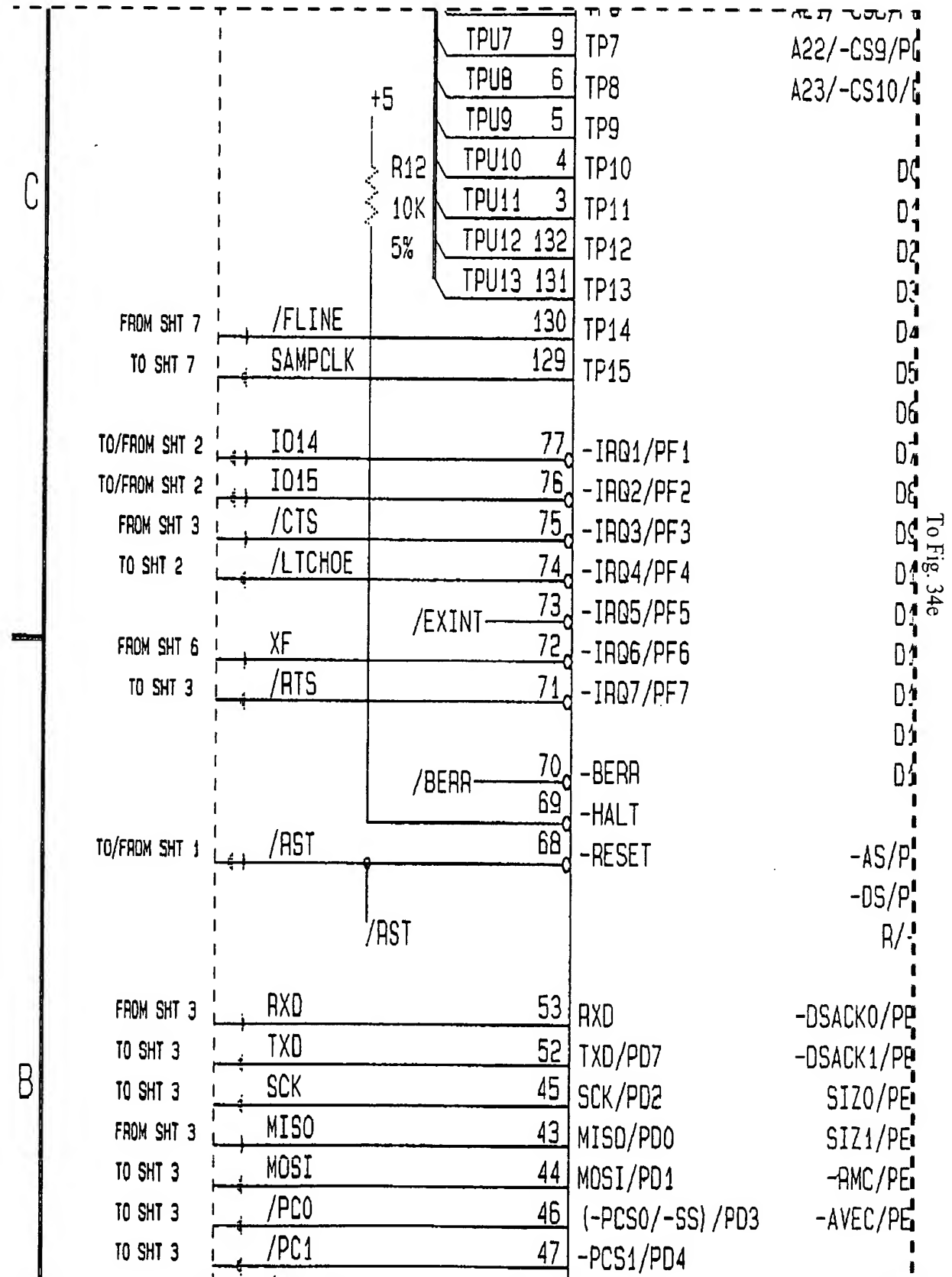
FIG. 34b



To Fig. 34f

FIG. 34c

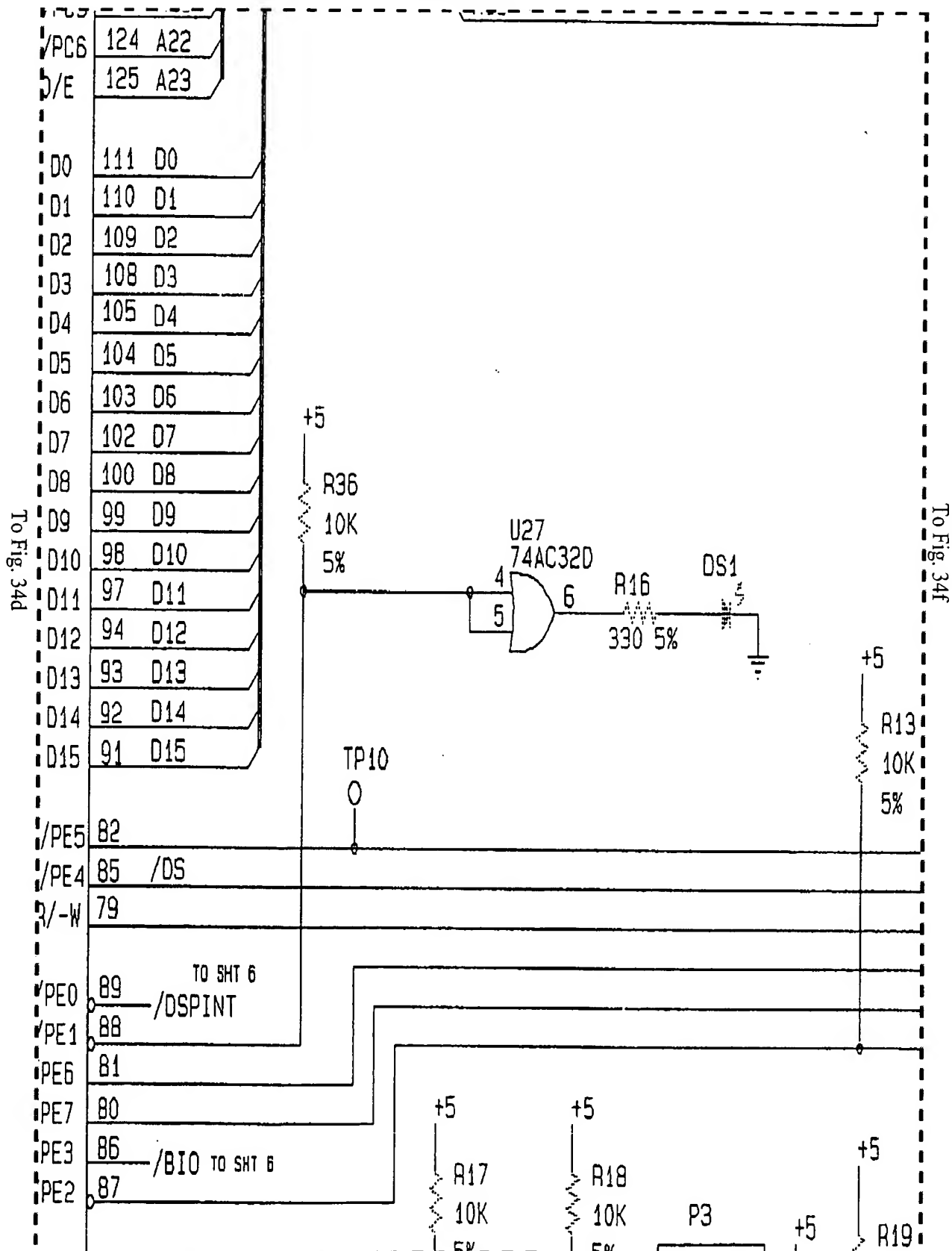
To Fig. 34a



To Fig. 34g

FIG. 34d

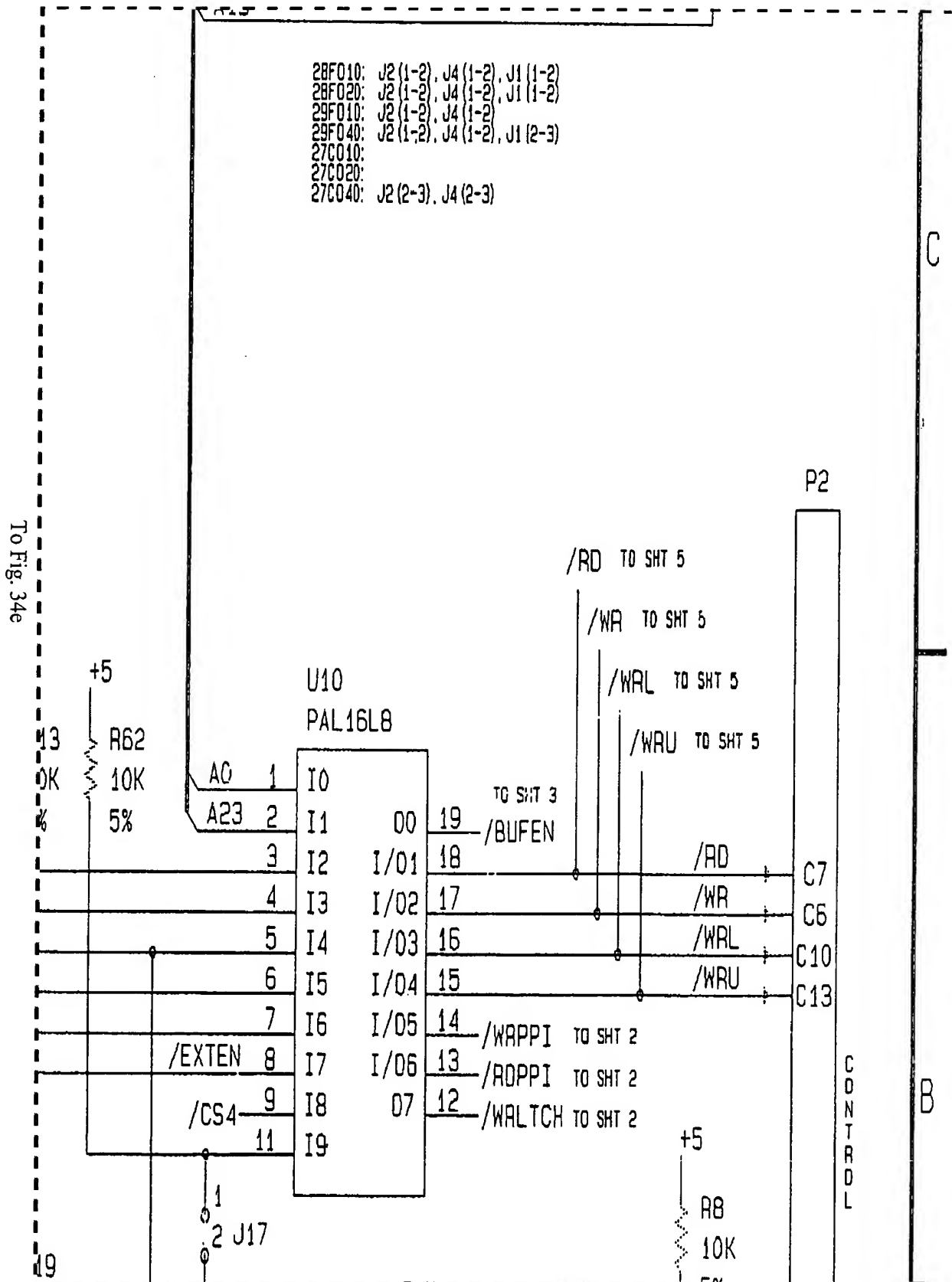
To Fig. 34b



To Fig. 34h

FIG. 34e

To Fig. 34c



To Fig. 34i

FIG. 34f

To Fig. 34d

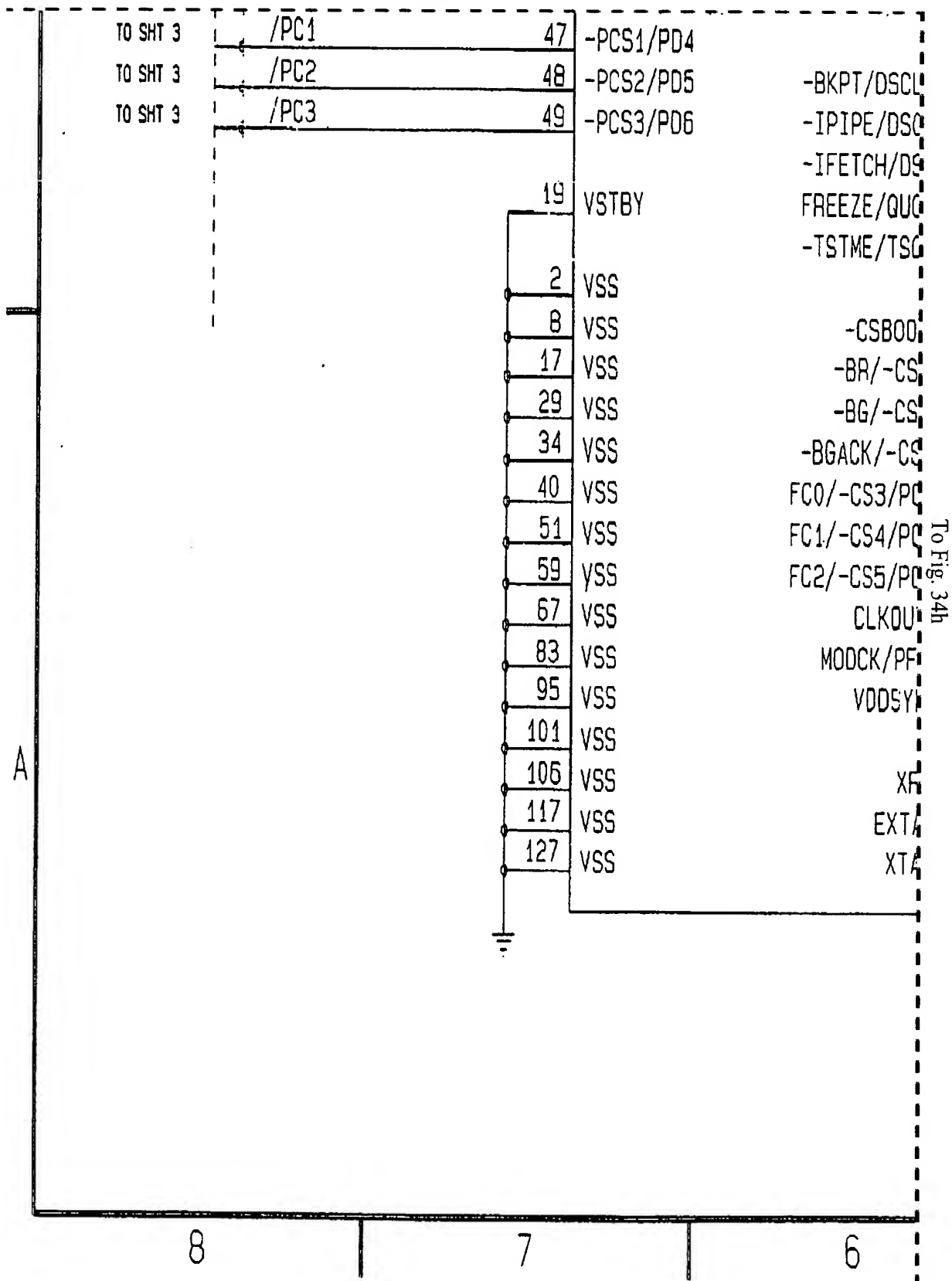


FIG. 34g

To Fig. 34e

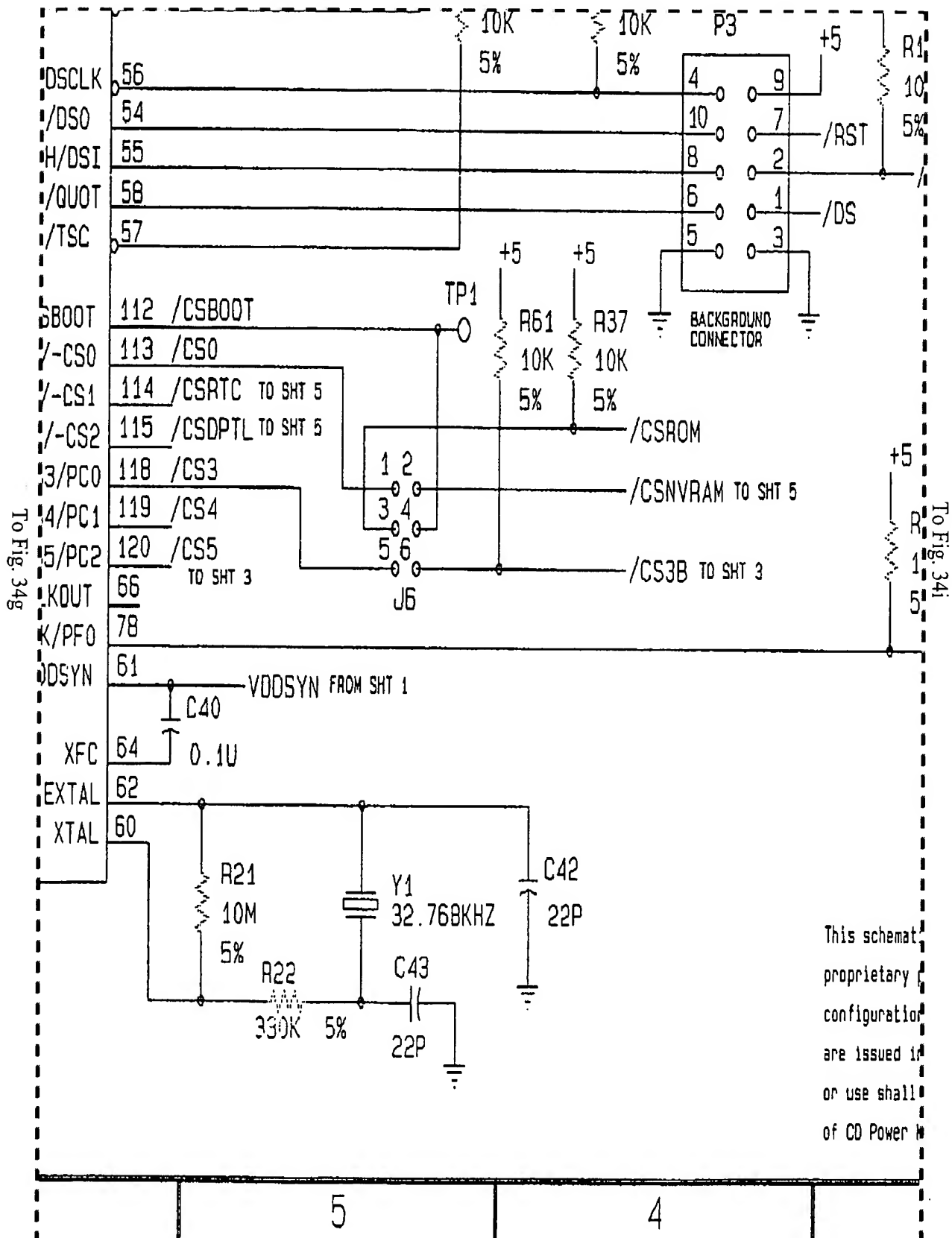


FIG. 34h

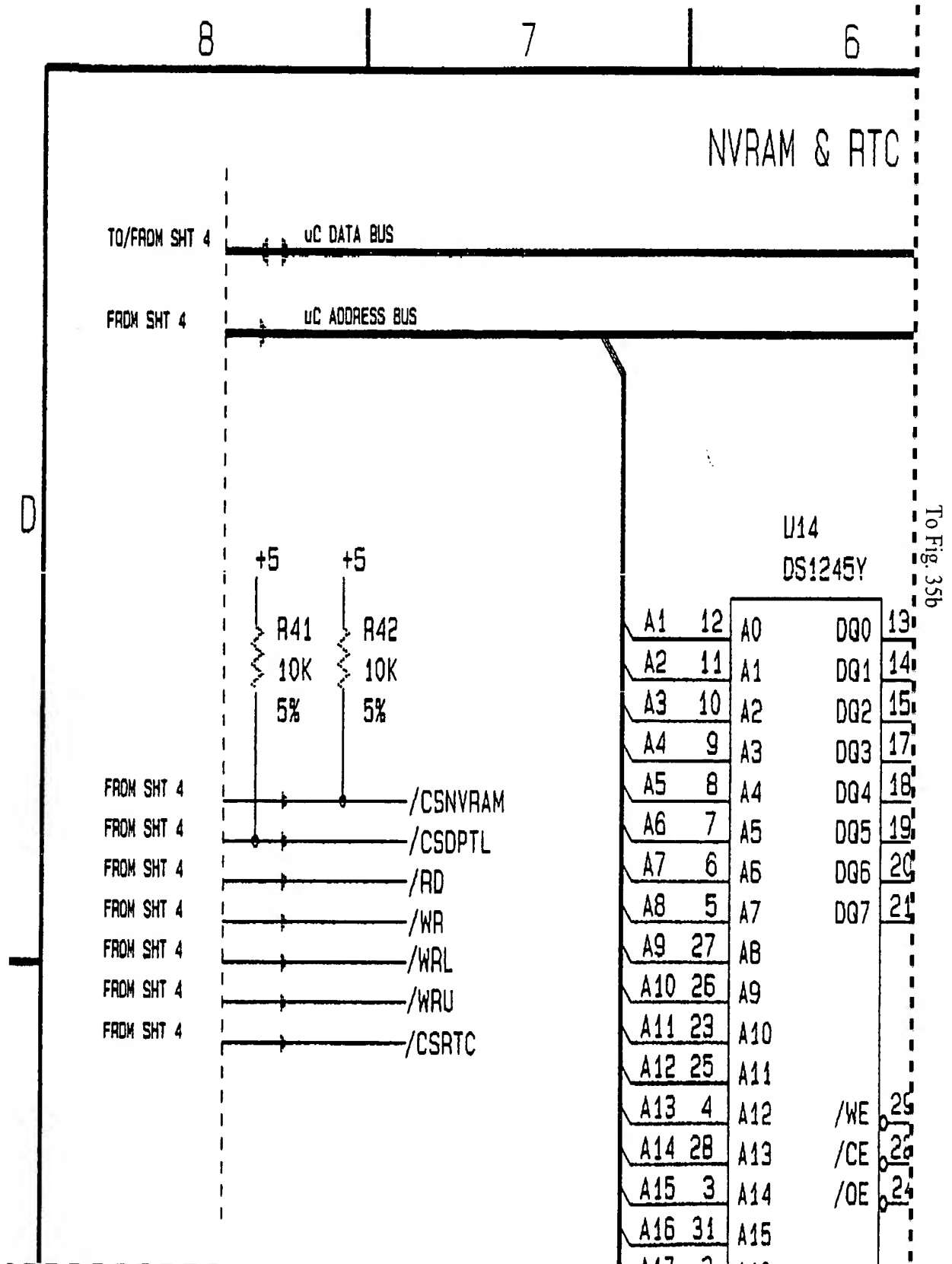
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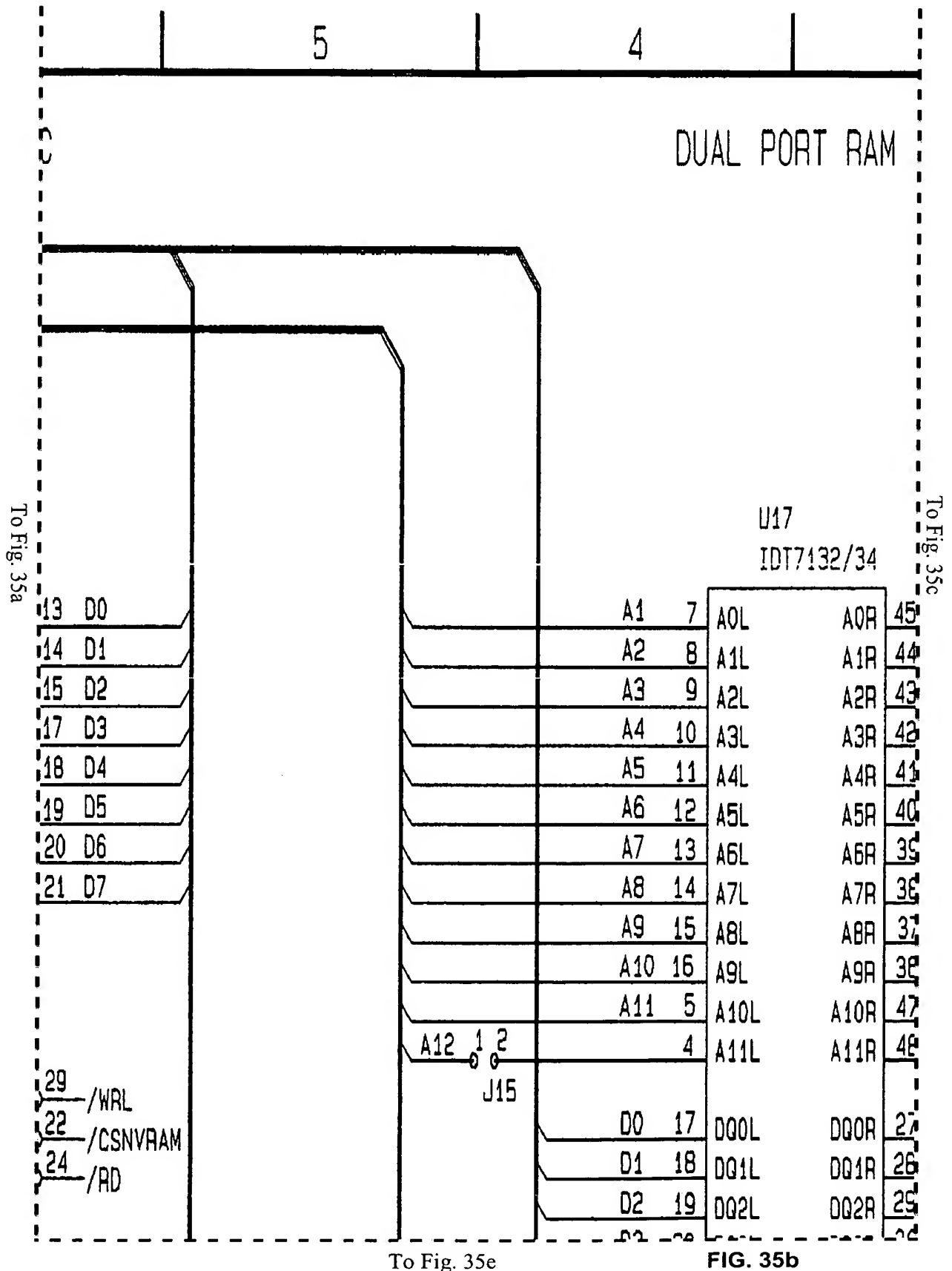
3 2 1

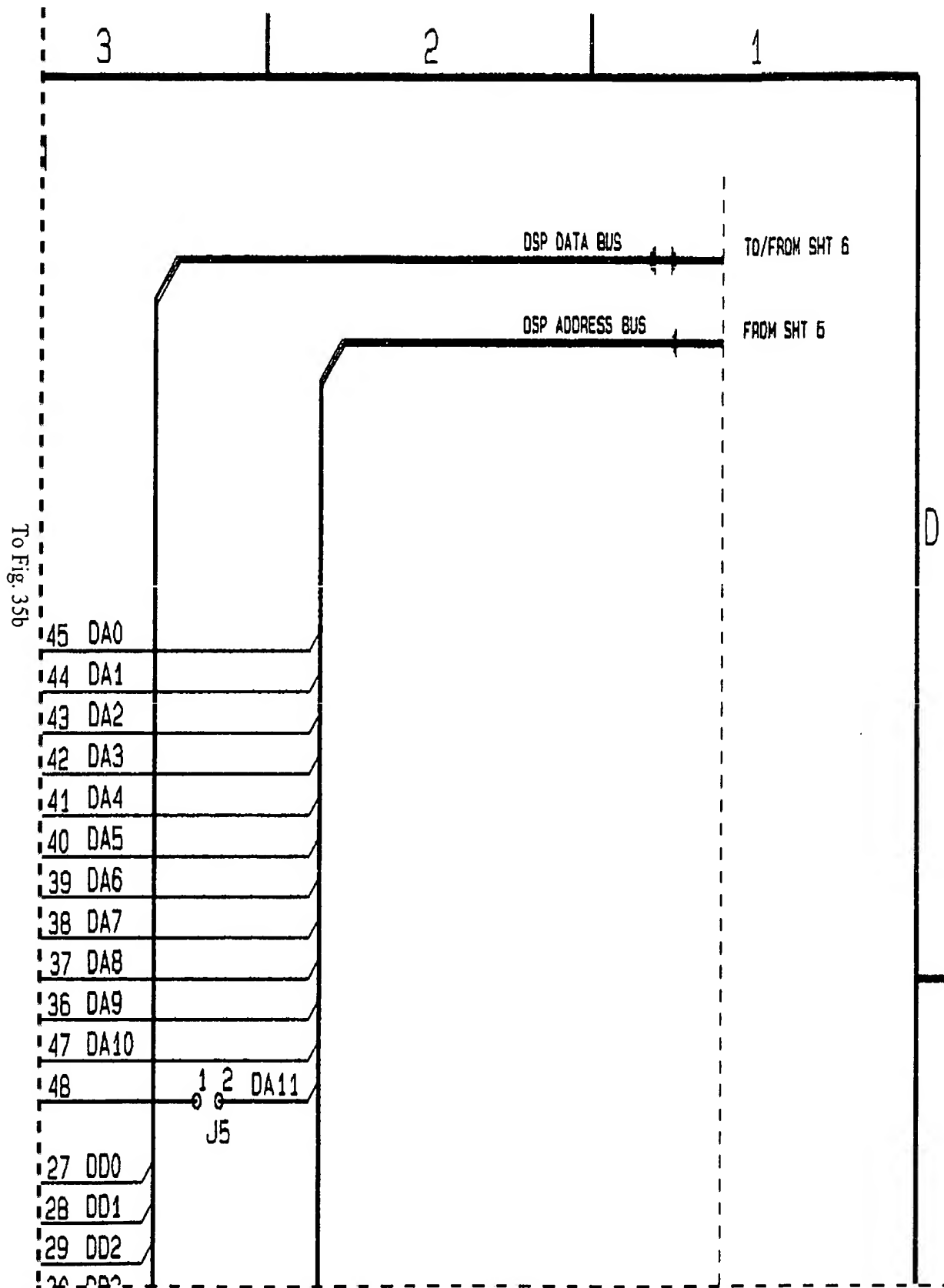
FIG. 34i



To Fig. 35d

FIG. 35a

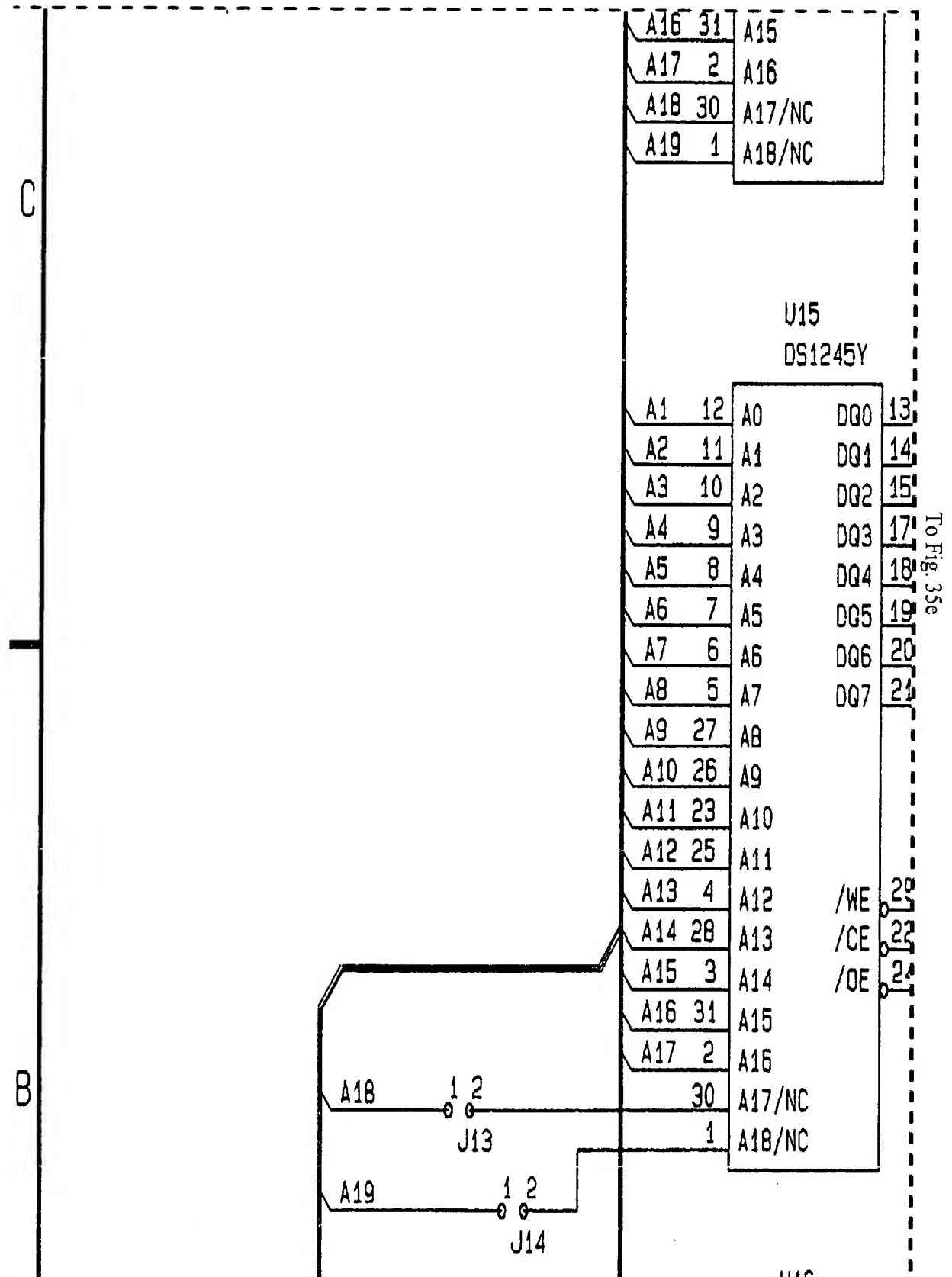




To Fig. 35f

FIG. 35c

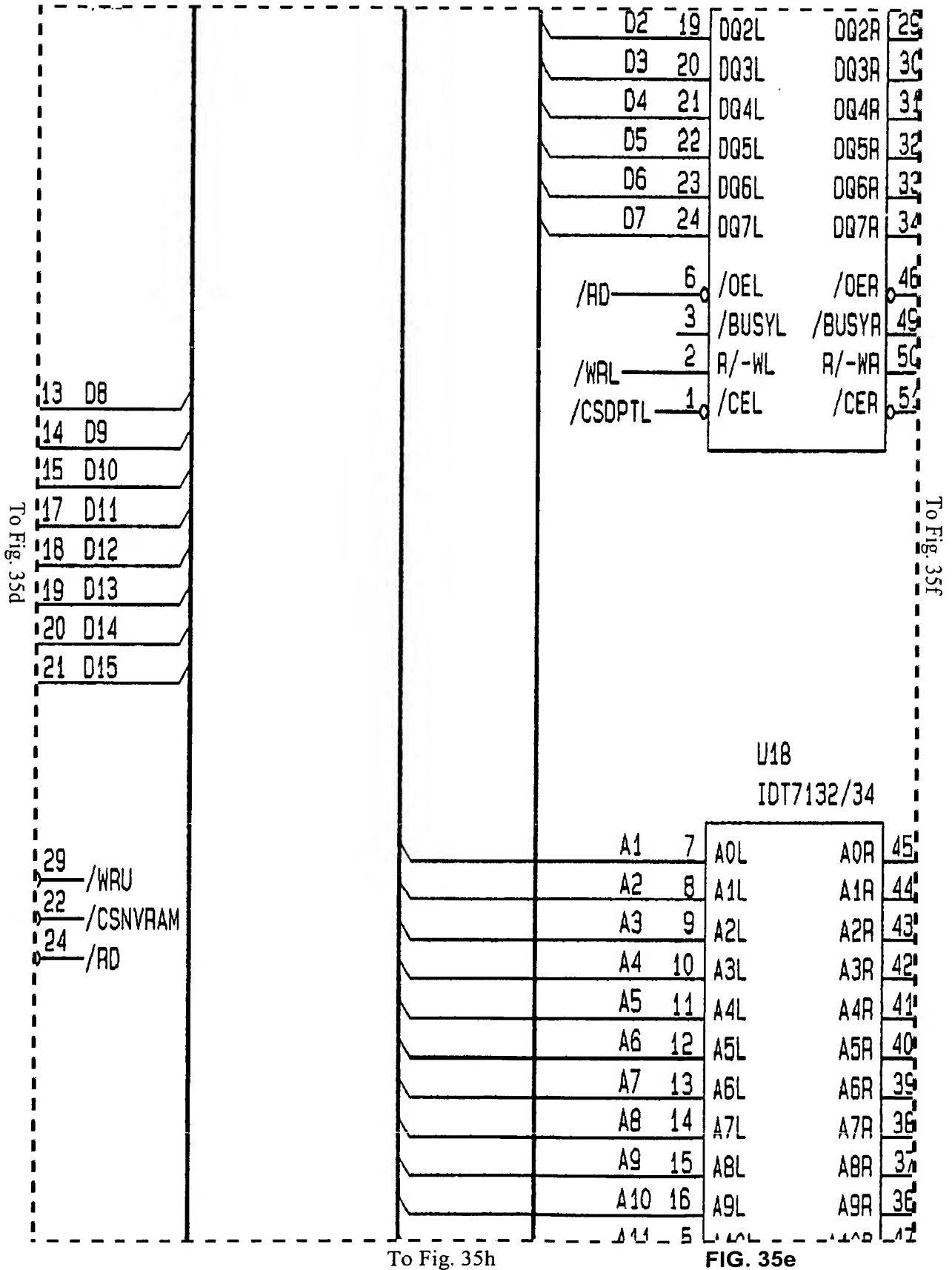
To Fig. 35a



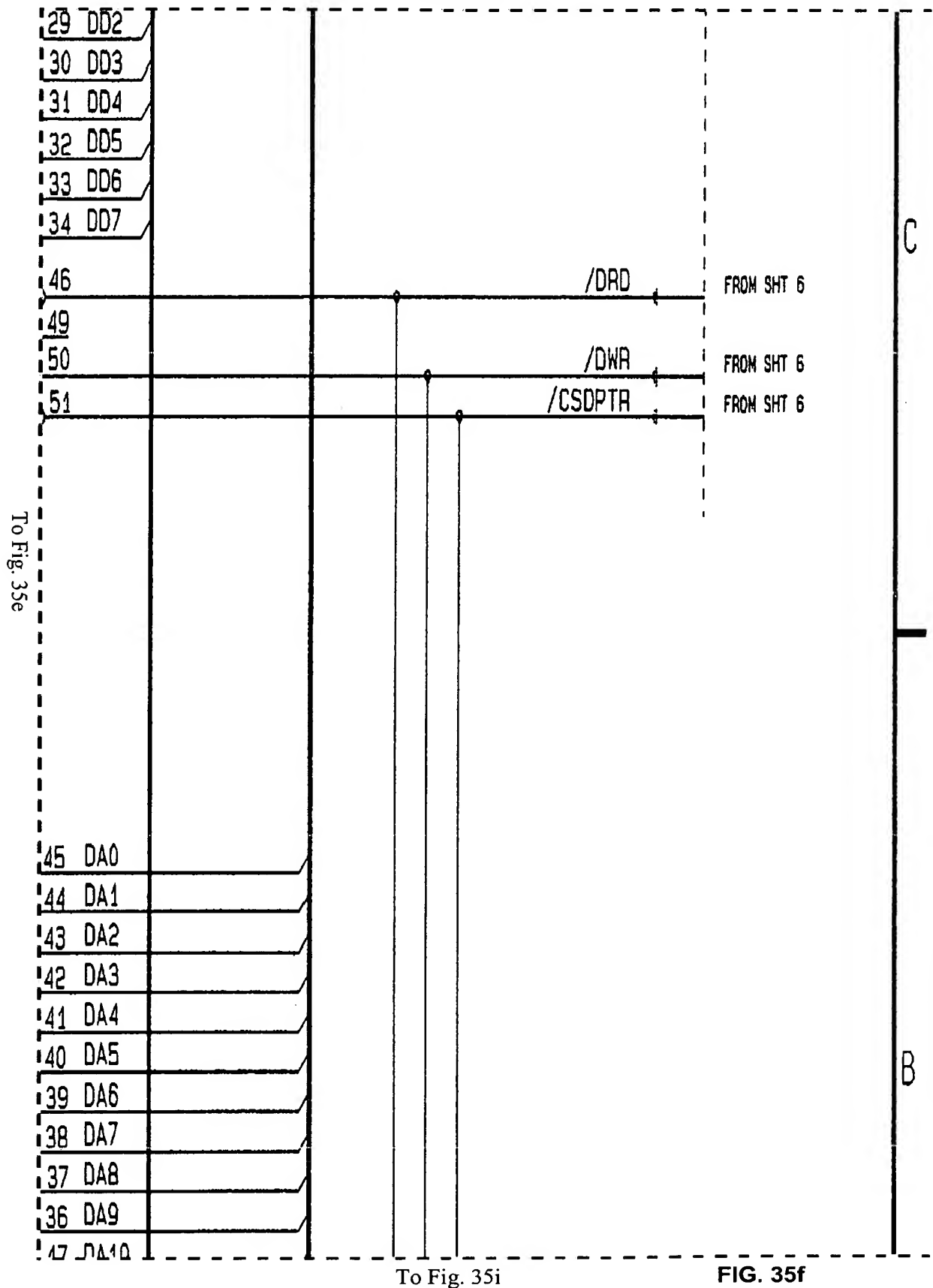
To Fig. 35g

FIG. 35d

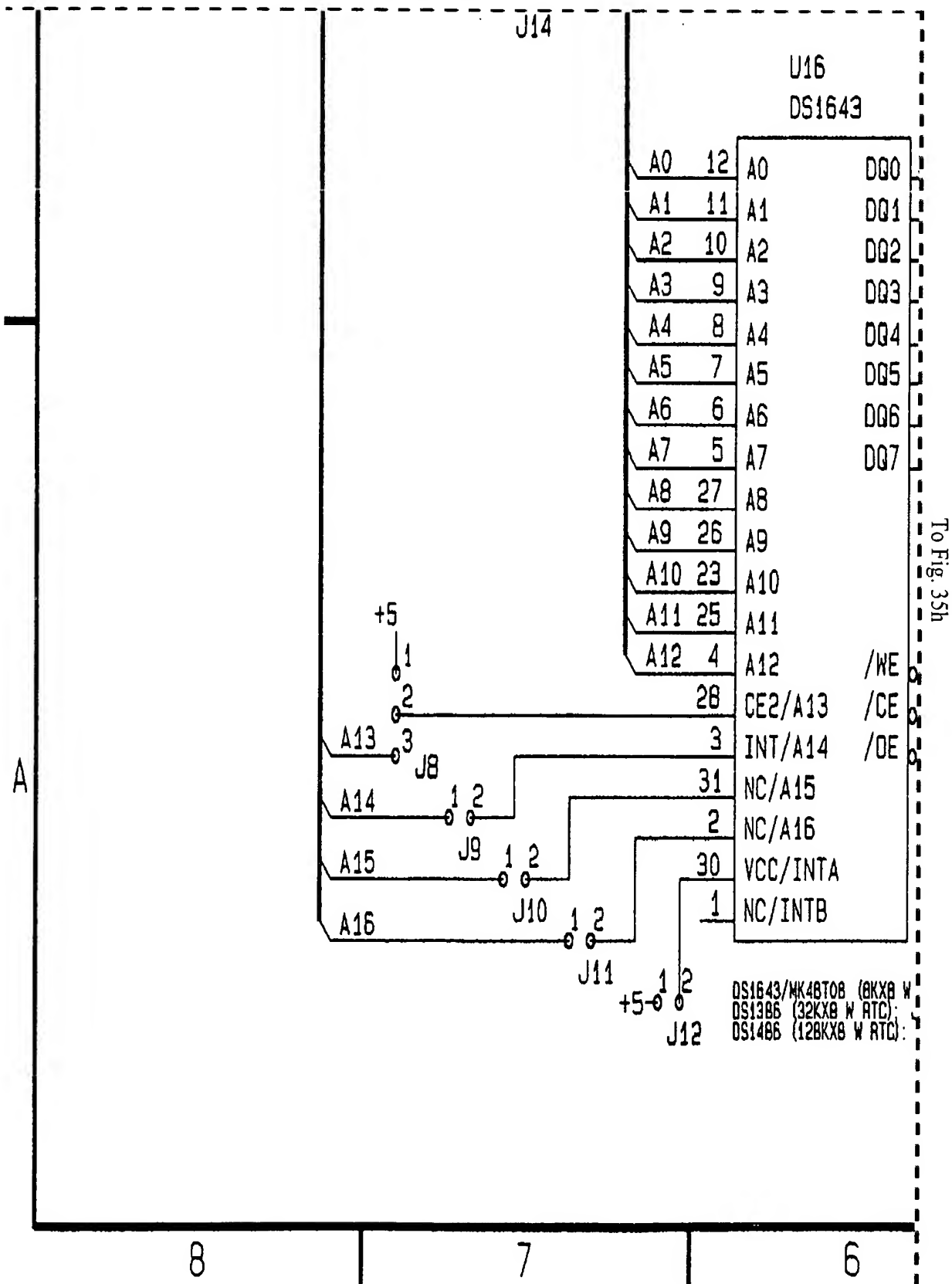
To Fig. 35b



To Fig. 35c



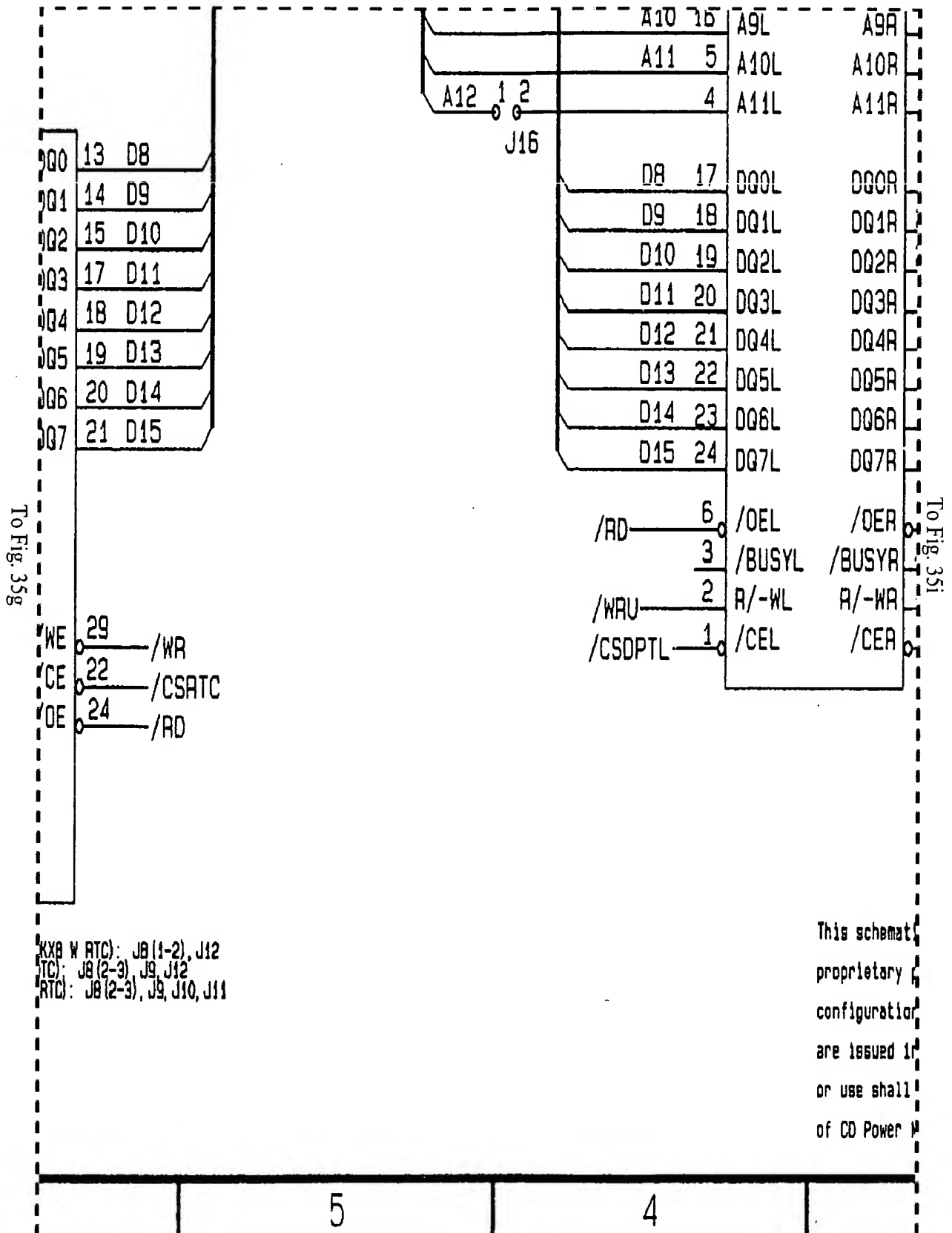
To Fig. 35d



To Fig. 35h

FIG. 35g

To Fig. 35e



KX8 W RTC): J8 (1-2), J12
 RTC): J8 (2-3), J9, J12
 RTC): J8 (2-3), J9, J10, J11

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To Fig. 35f

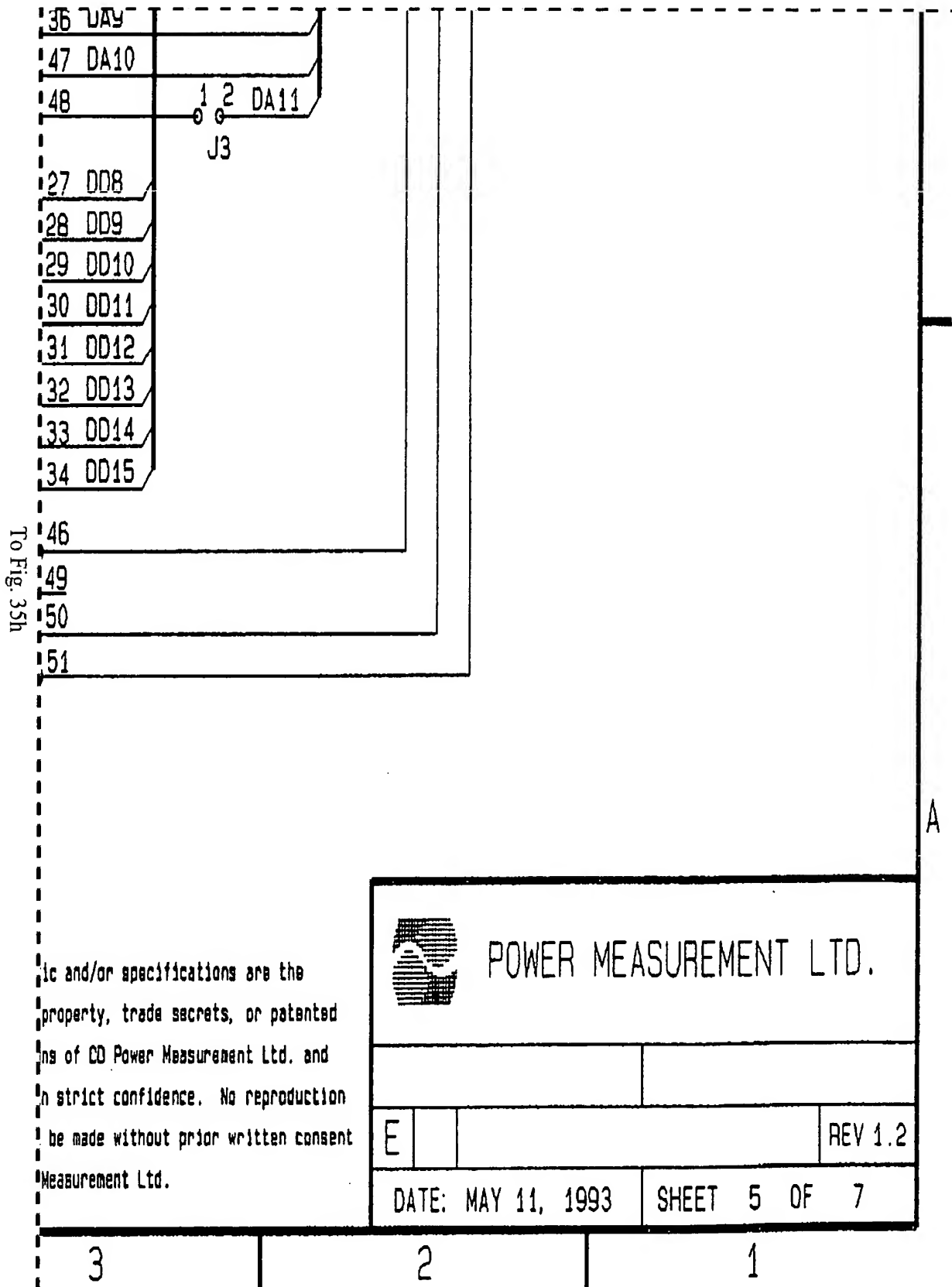
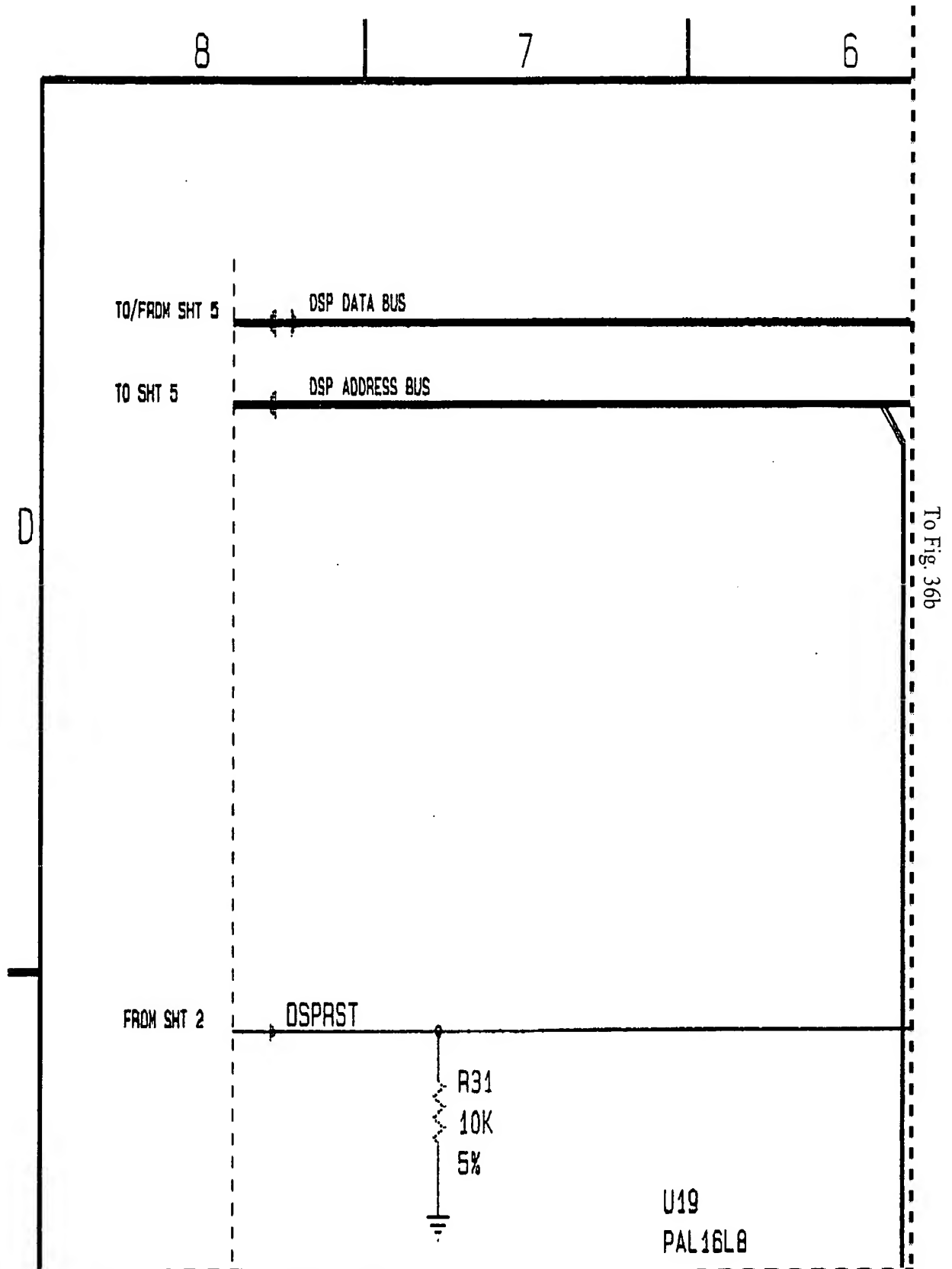
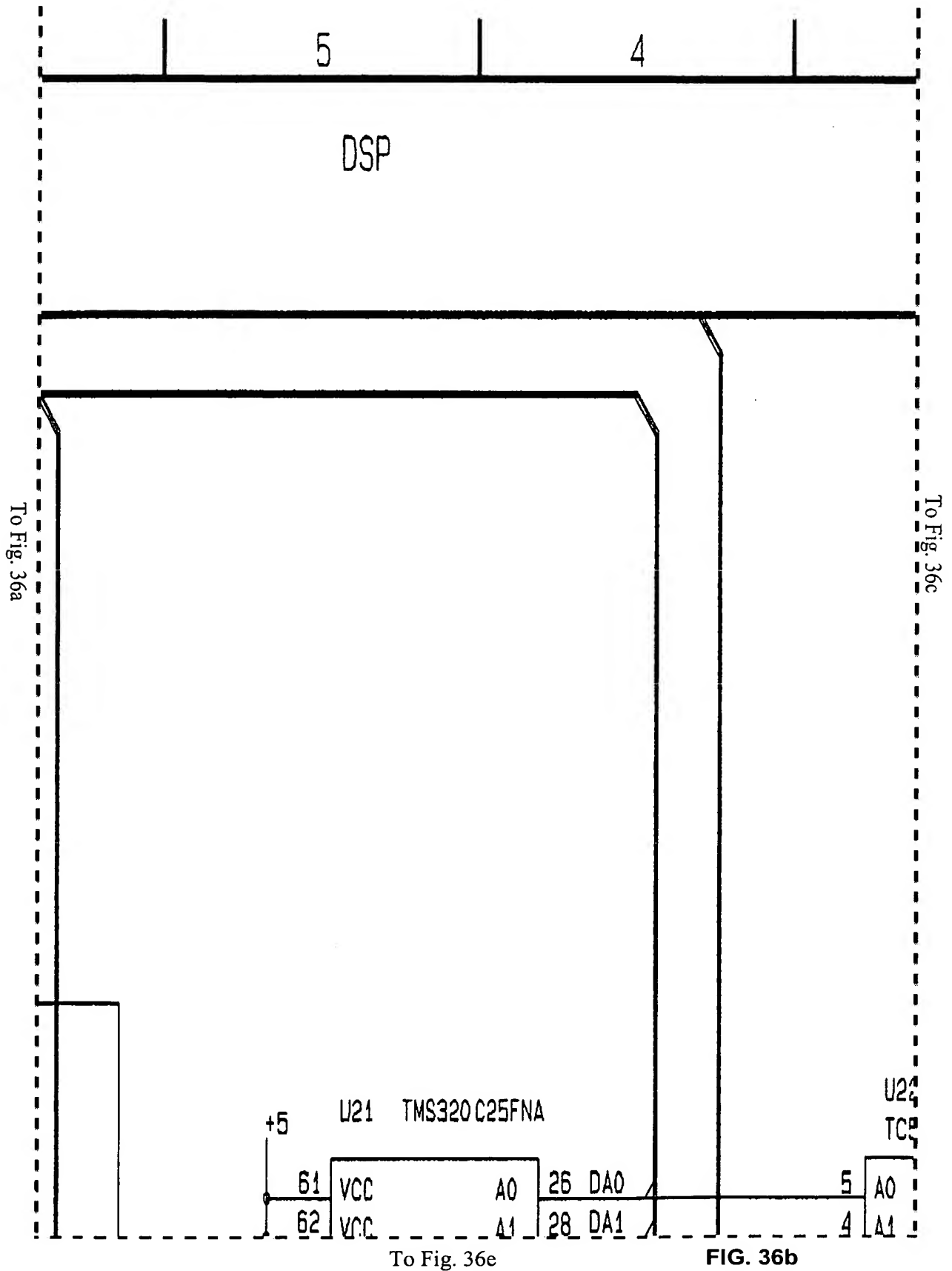


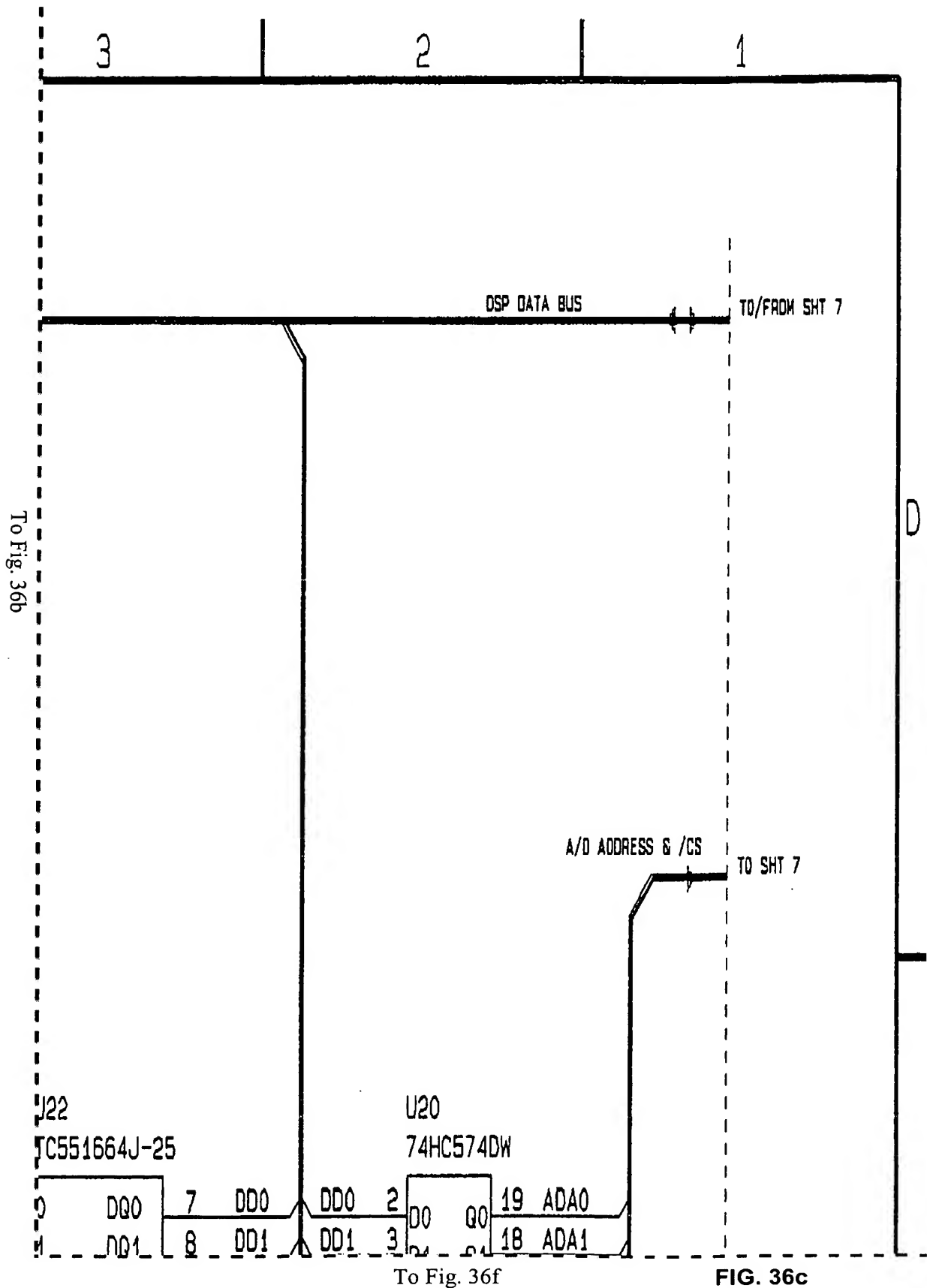
FIG. 35i



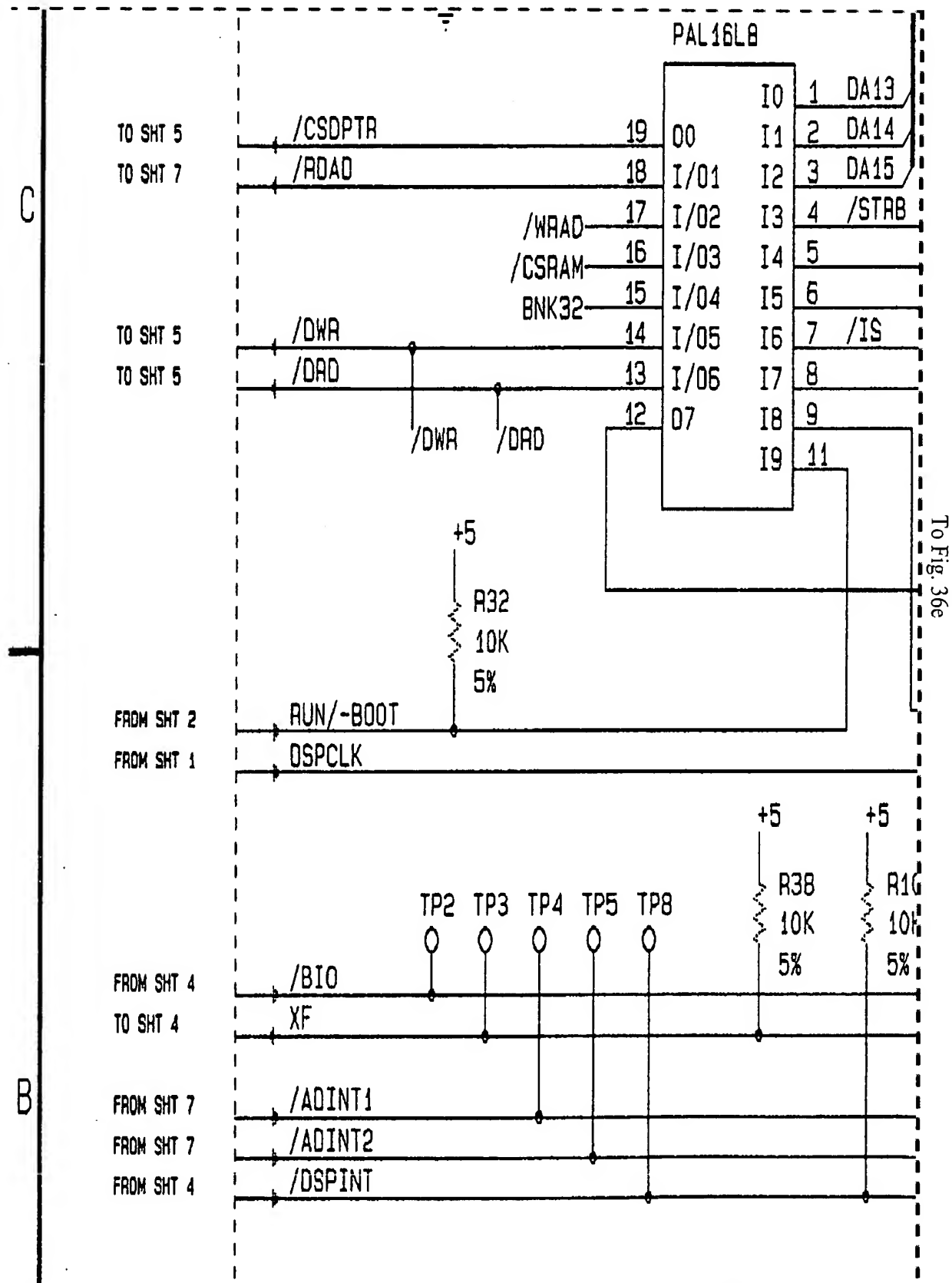
To Fig. 36d

FIG. 36a





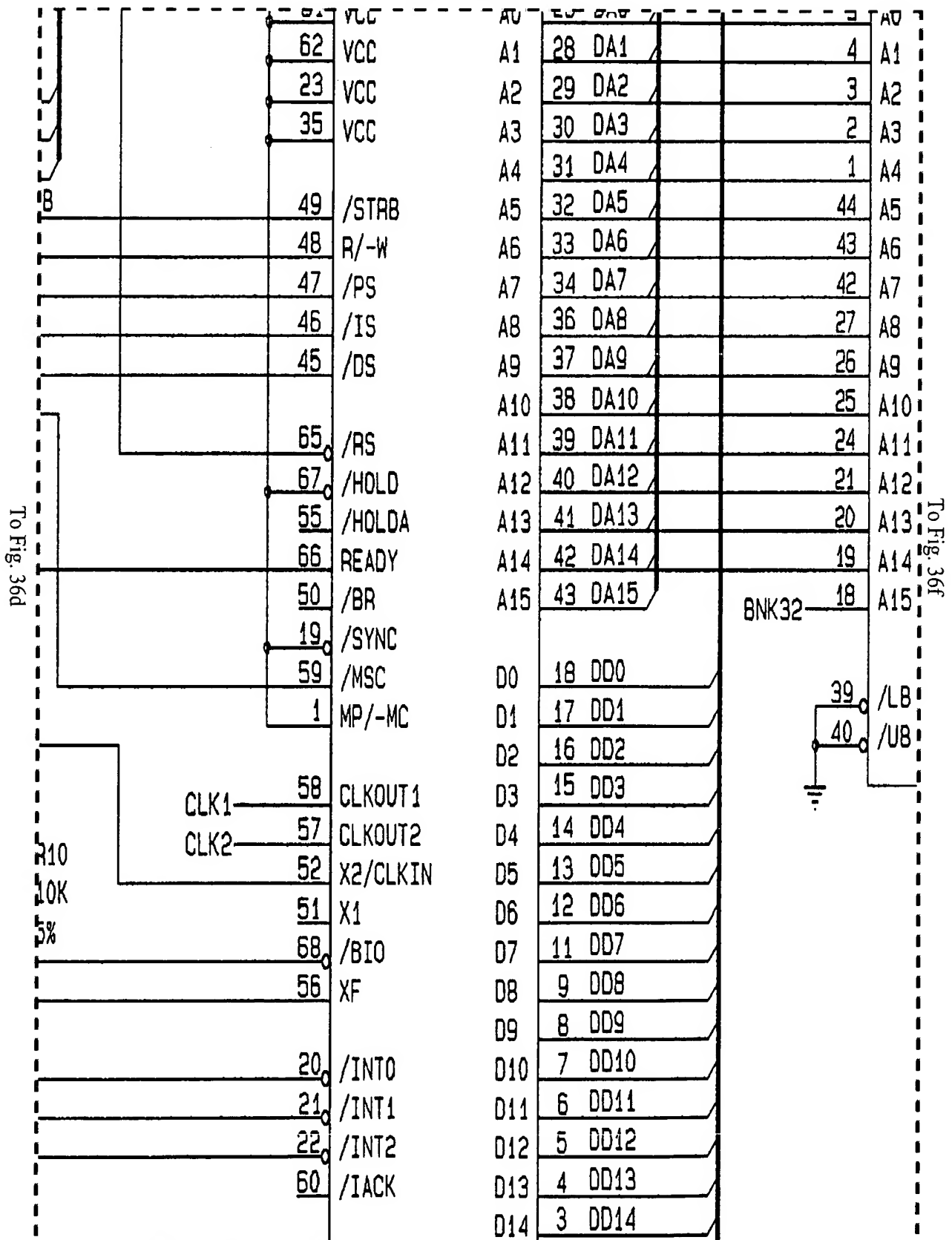
To Fig. 36a



To Fig. 36g

FIG. 36d

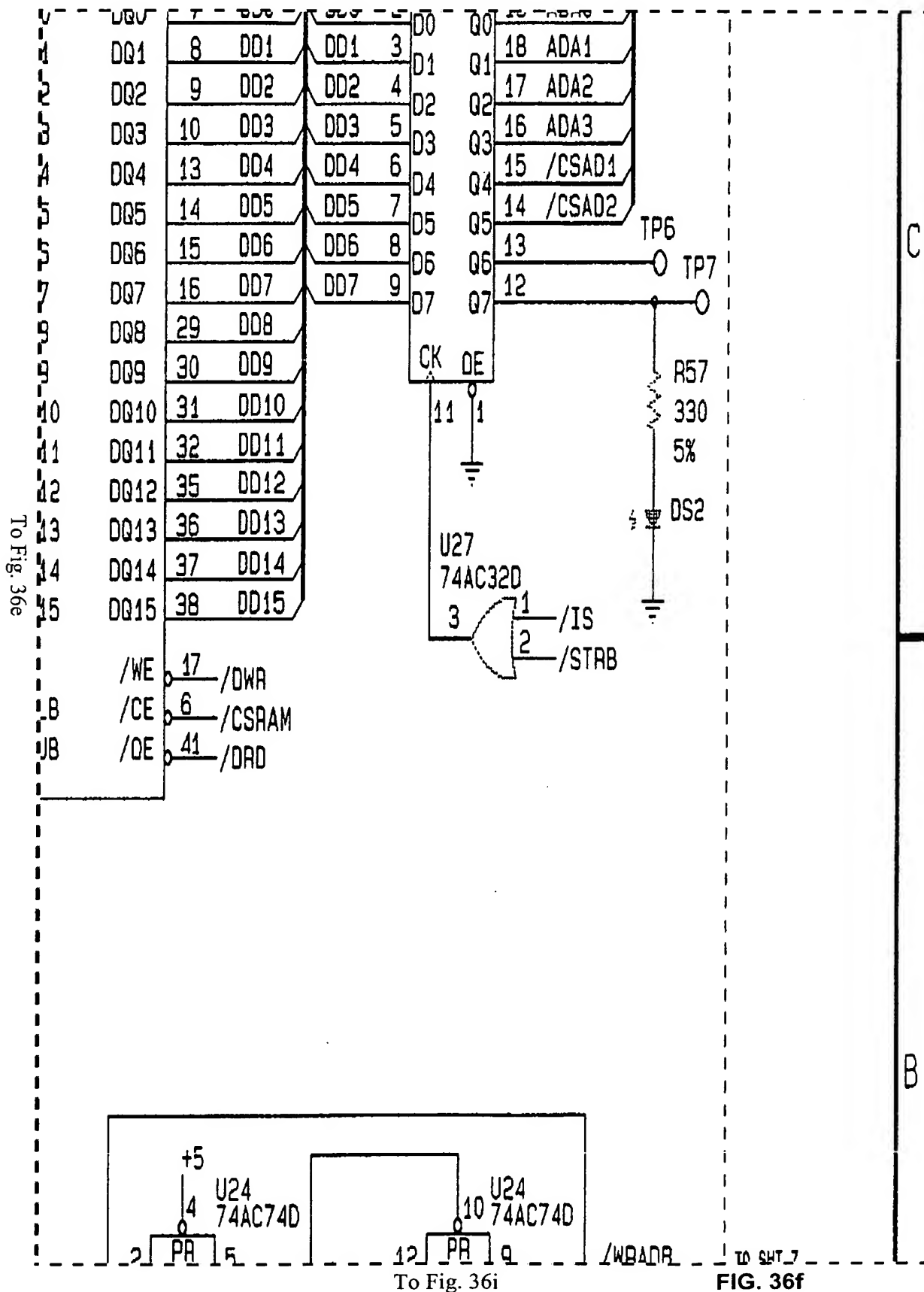
To Fig. 36b



To Fig. 36h

FIG. 36e

To Fig. 36c



To Fig. 36i

FIG. 36f

To Fig. 36d

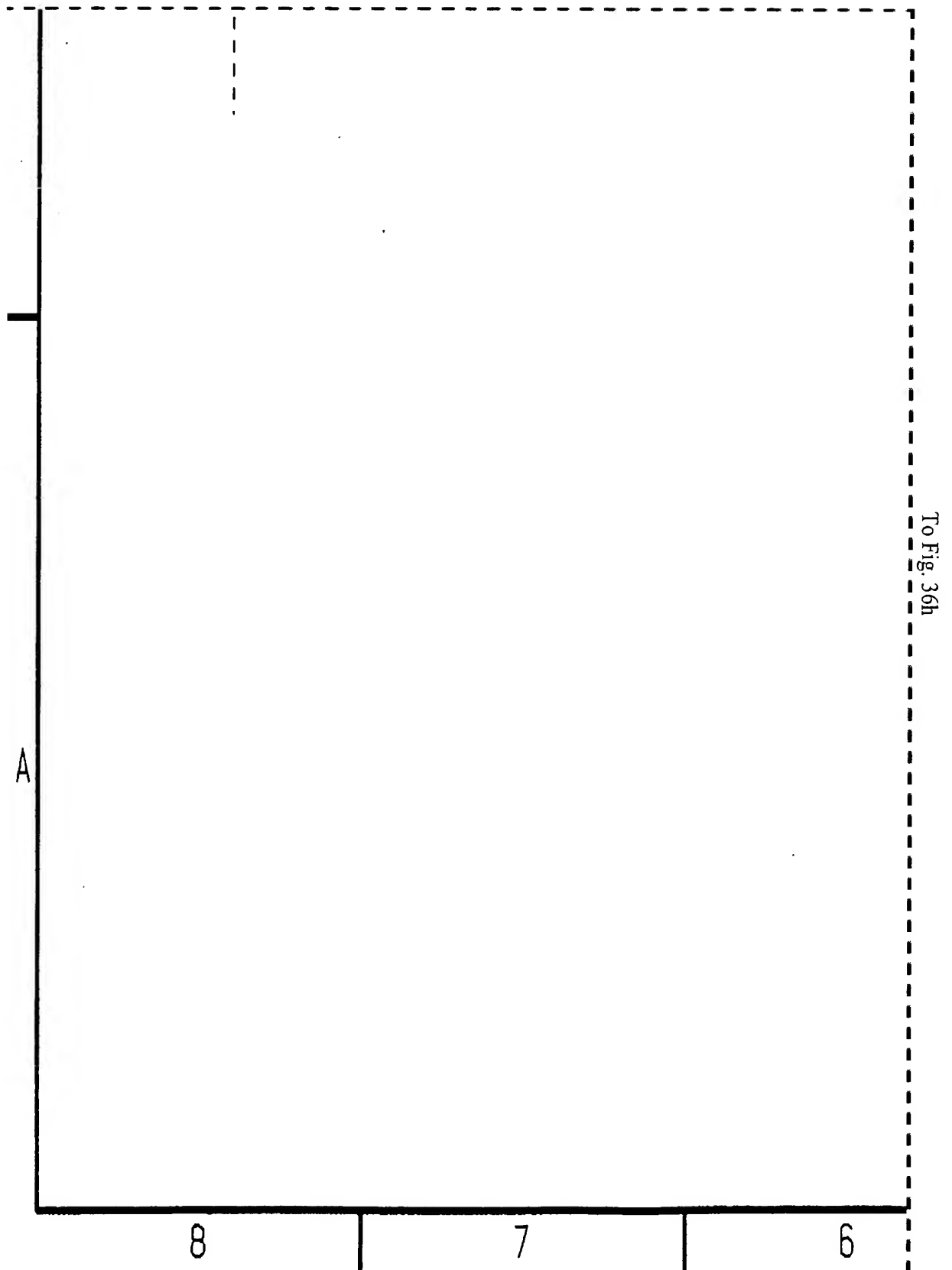
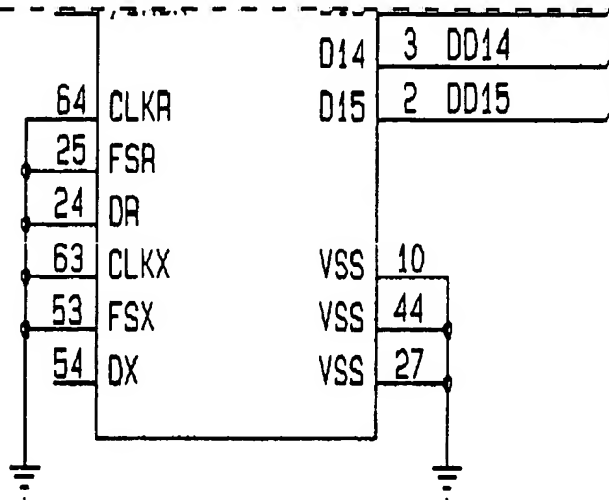


FIG. 36g

To Fig. 36e



To Fig. 36g

To Fig. 36i

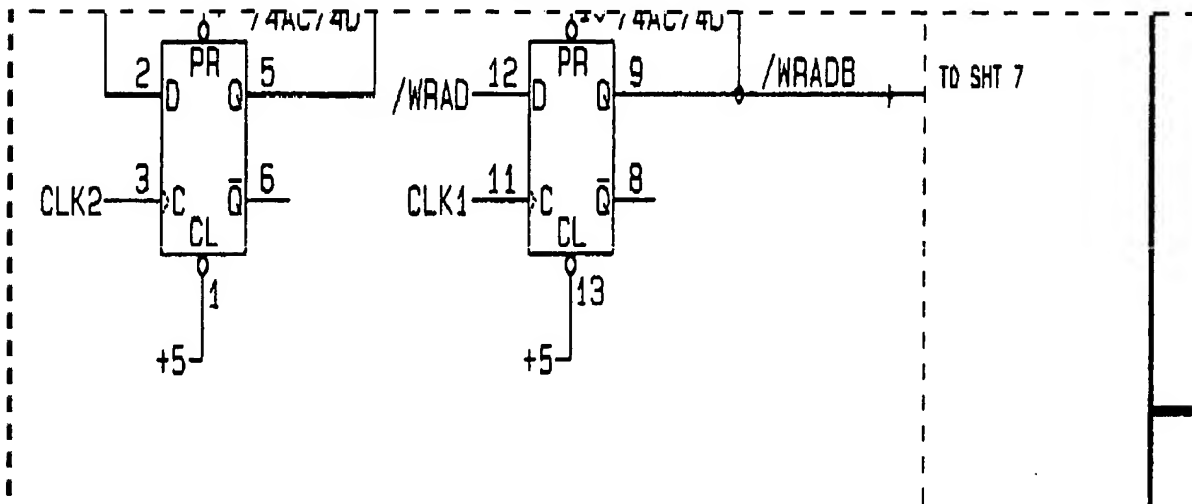
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FIG. 36h

To Fig. 36f



To Fig. 36h

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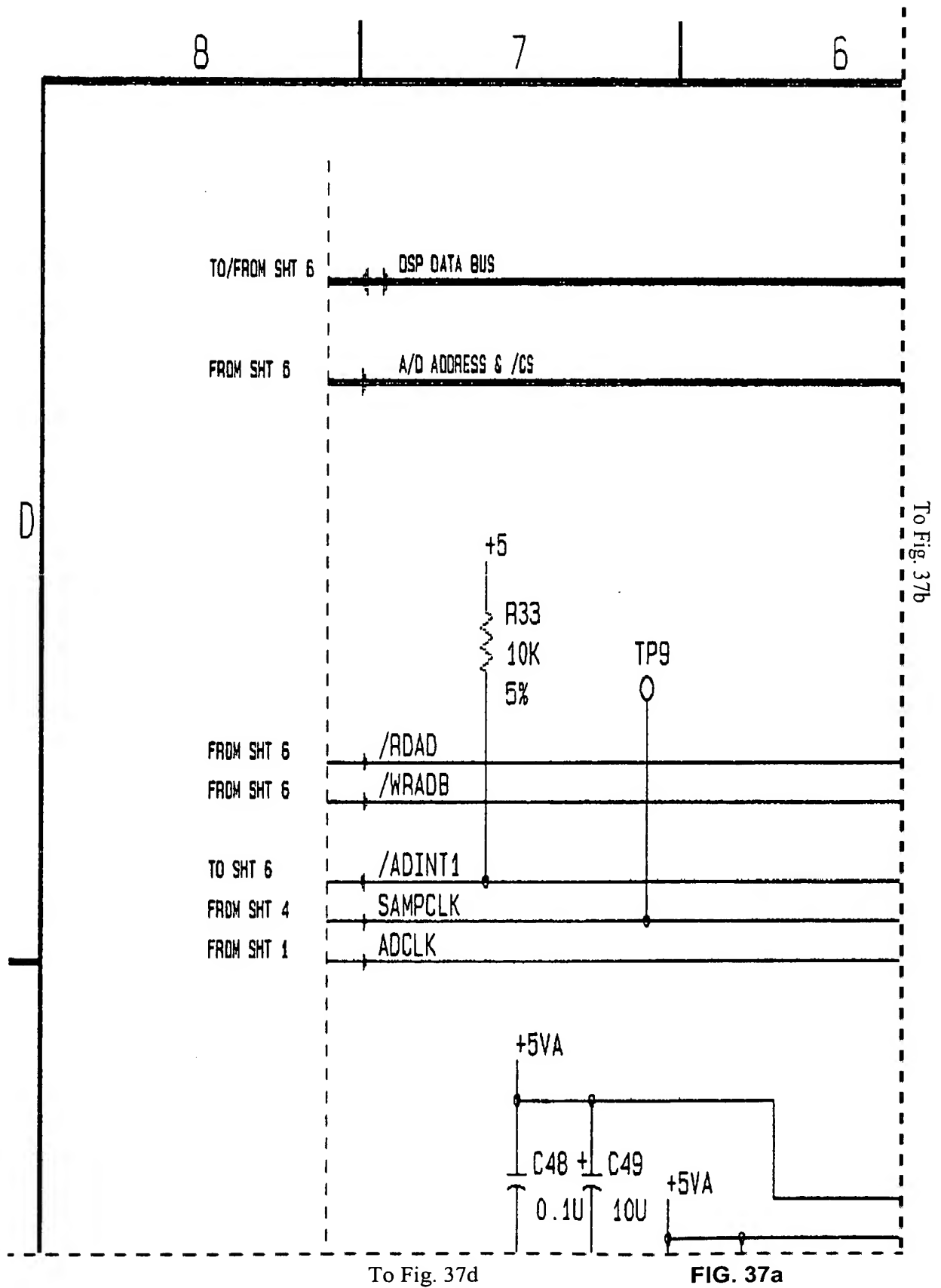
SHEET 6 OF 7

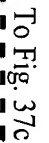
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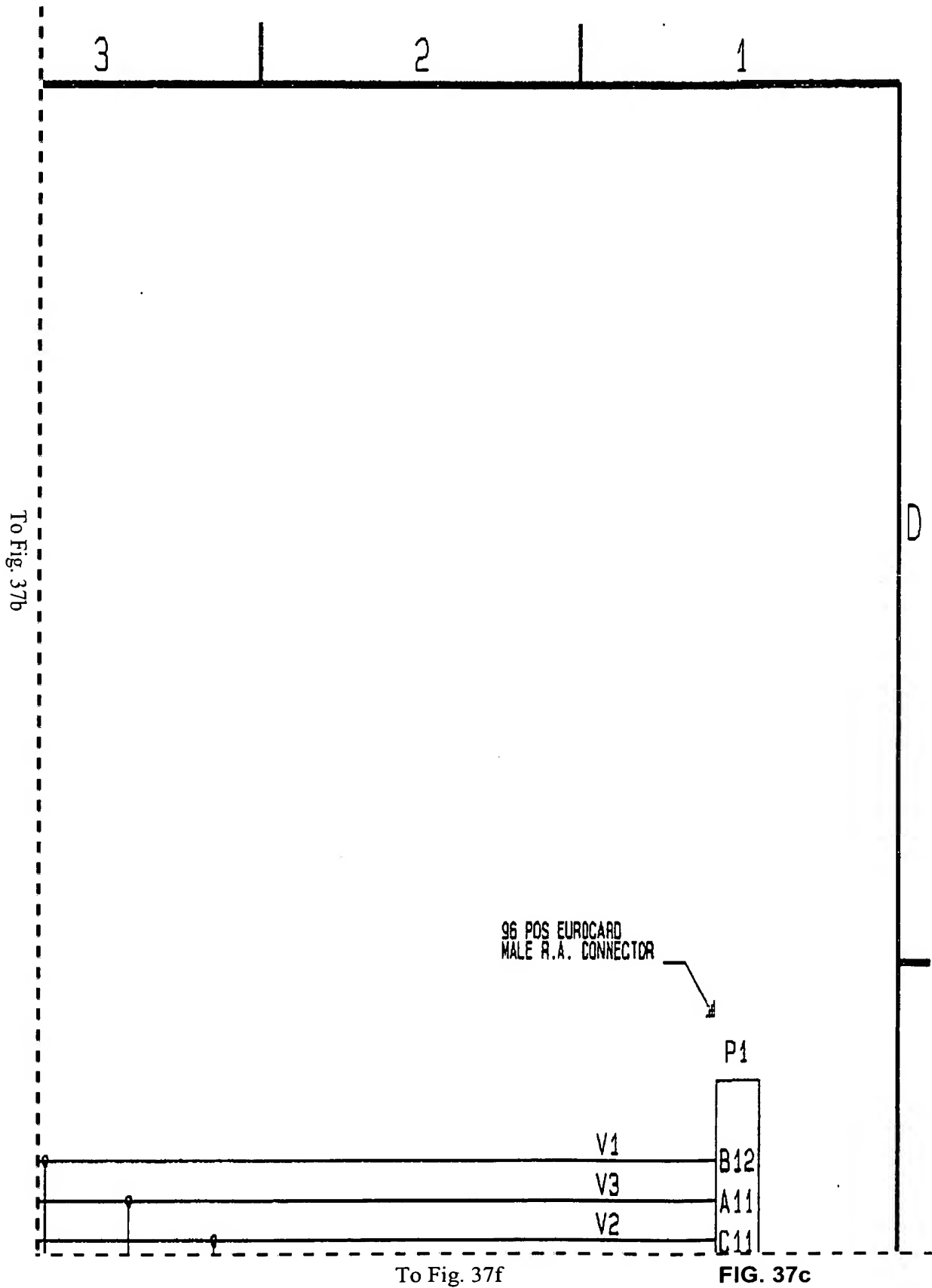
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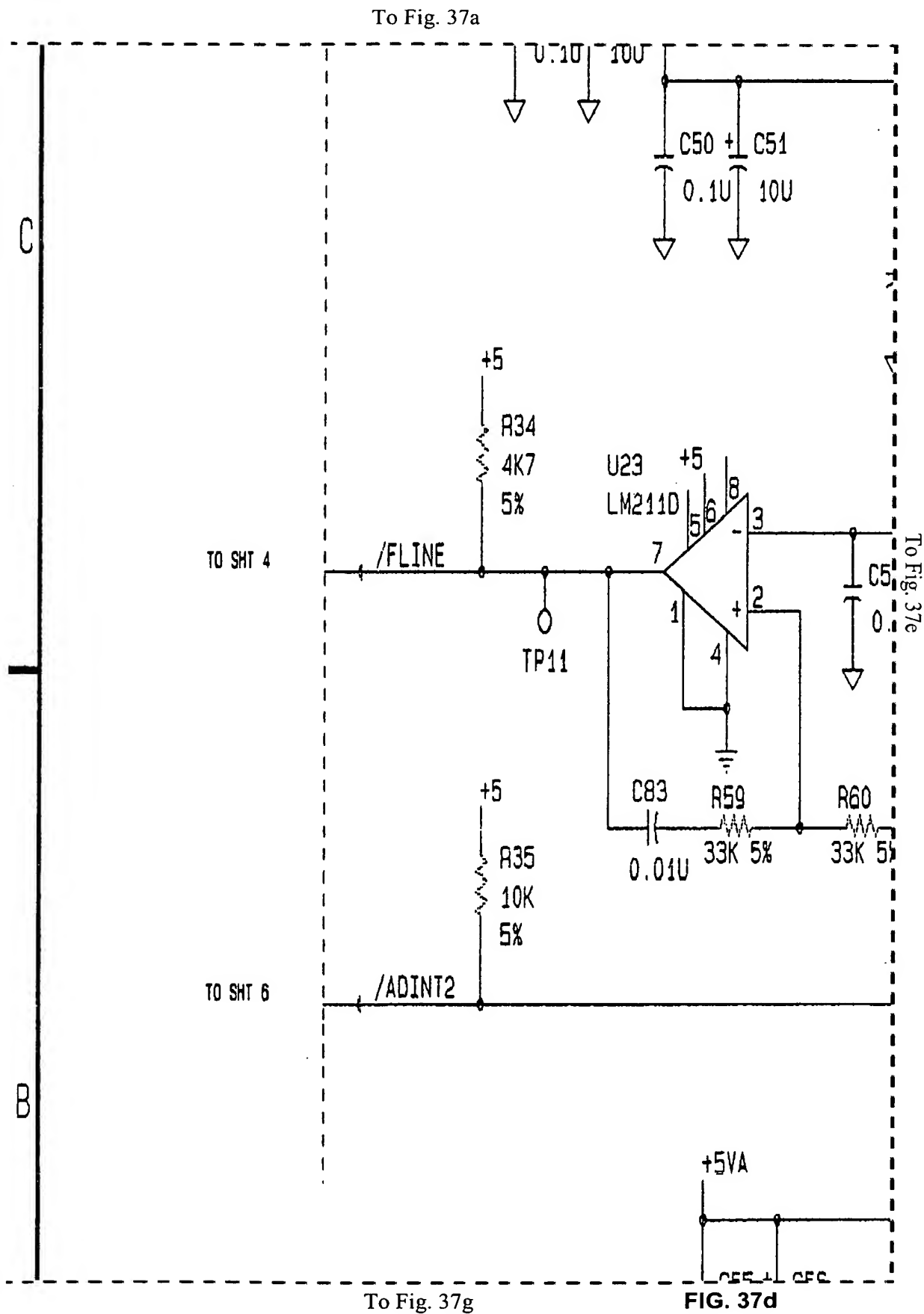
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FIG. 36i

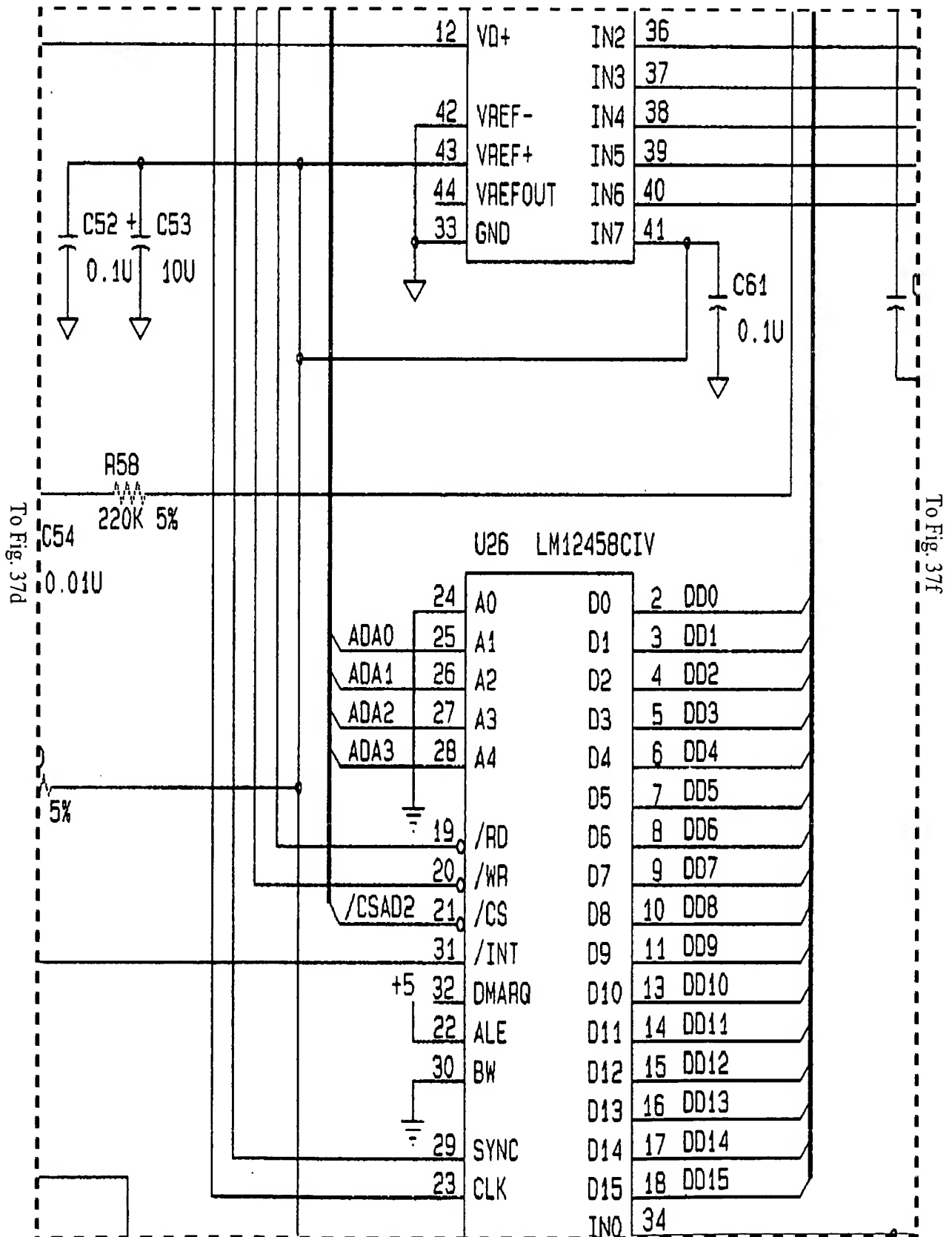








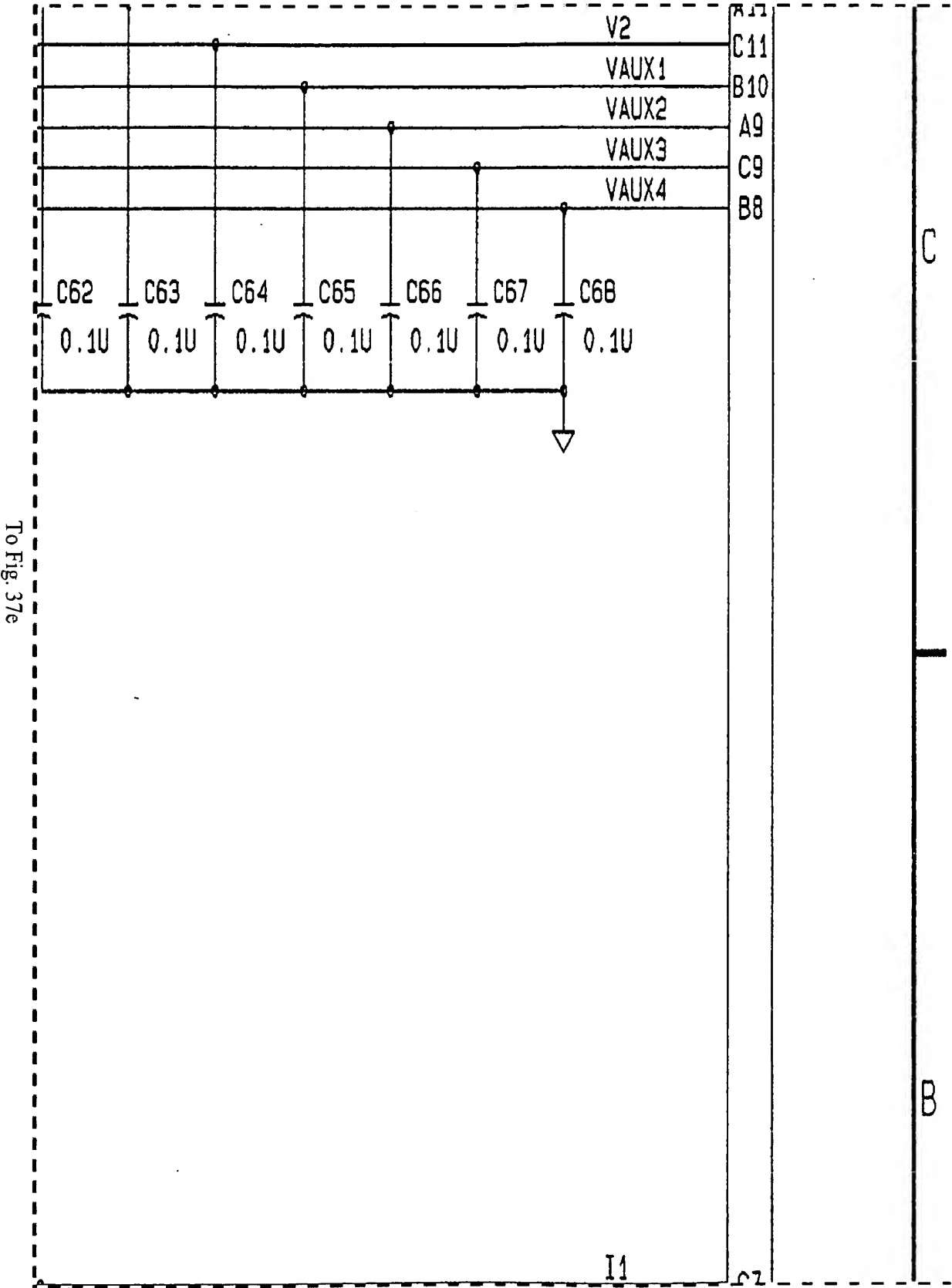
To Fig. 37b



To Fig. 37h

FIG. 37e

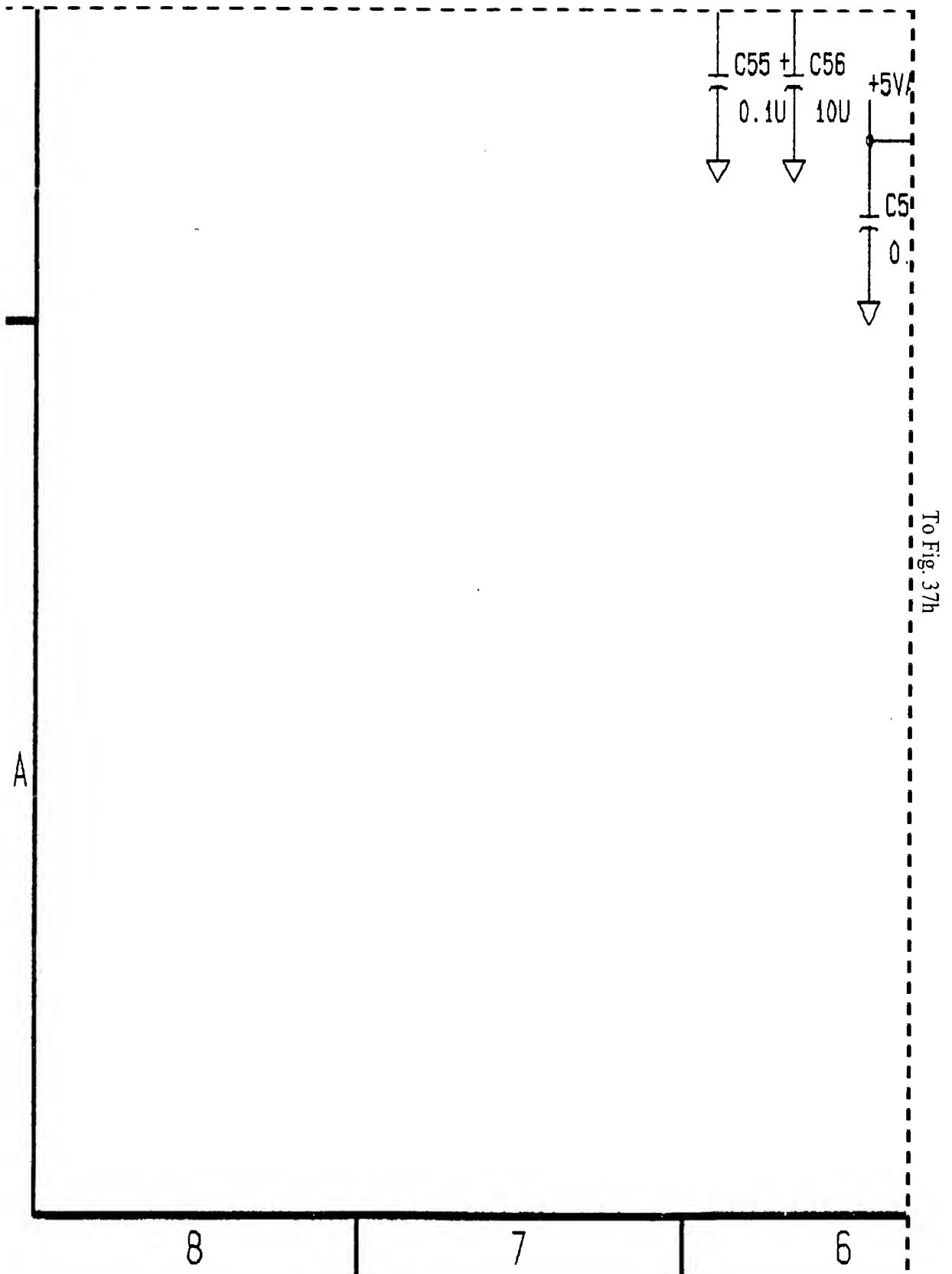
To Fig. 37c



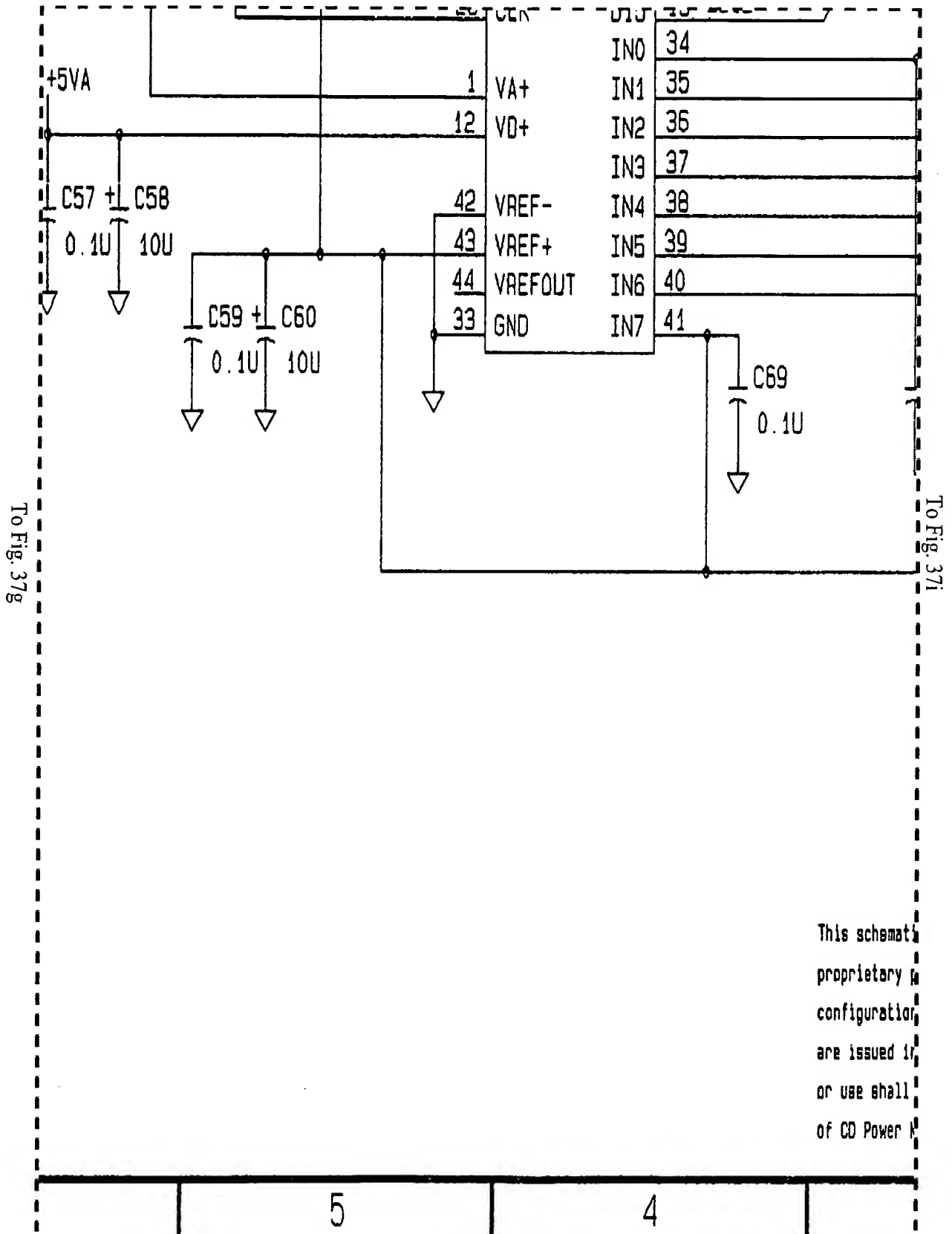
To Fig. 37i

FIG. 37f

To Fig. 37d



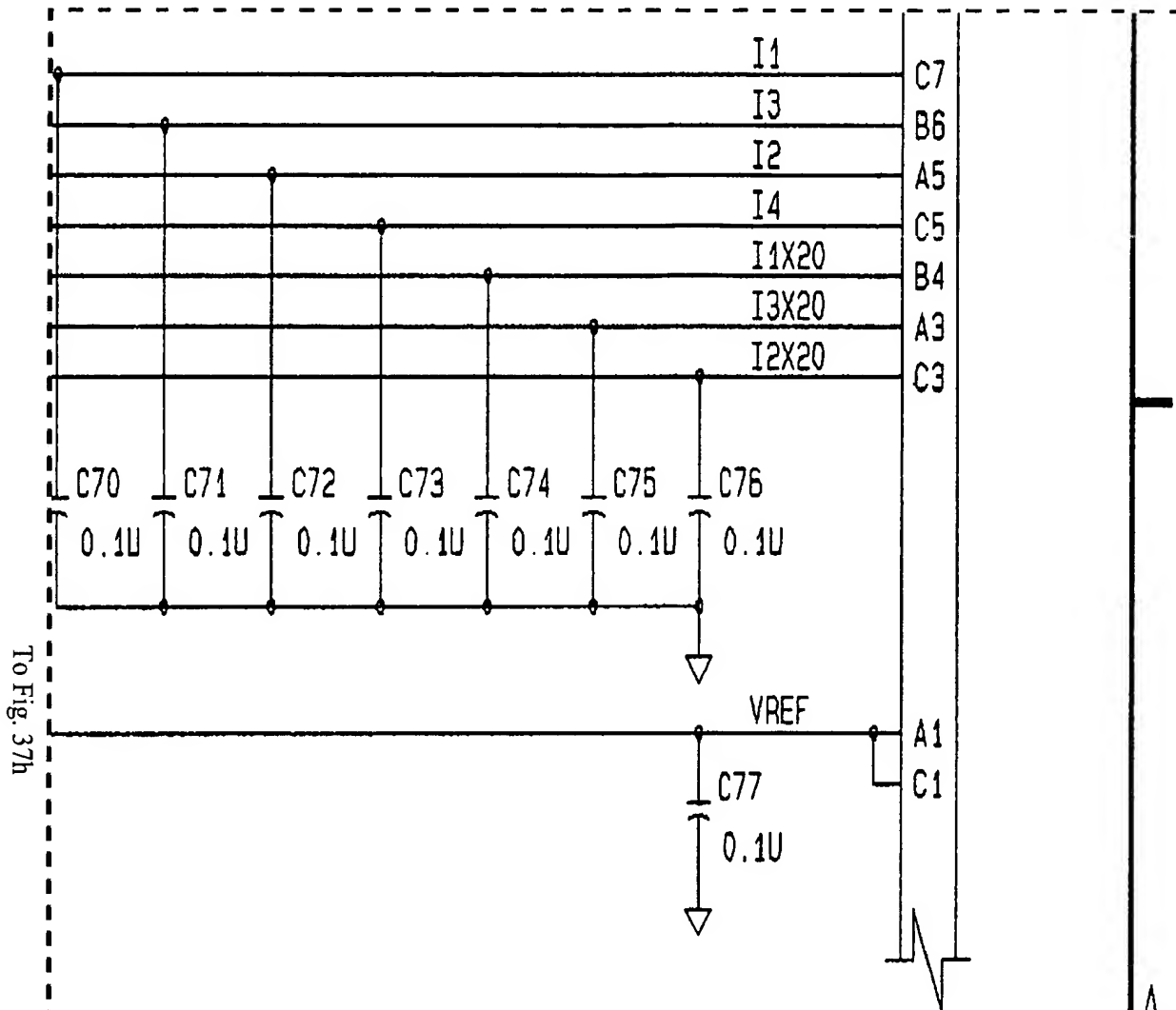
To Fig. 37e



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FIG. 37h

To Fig. 37f



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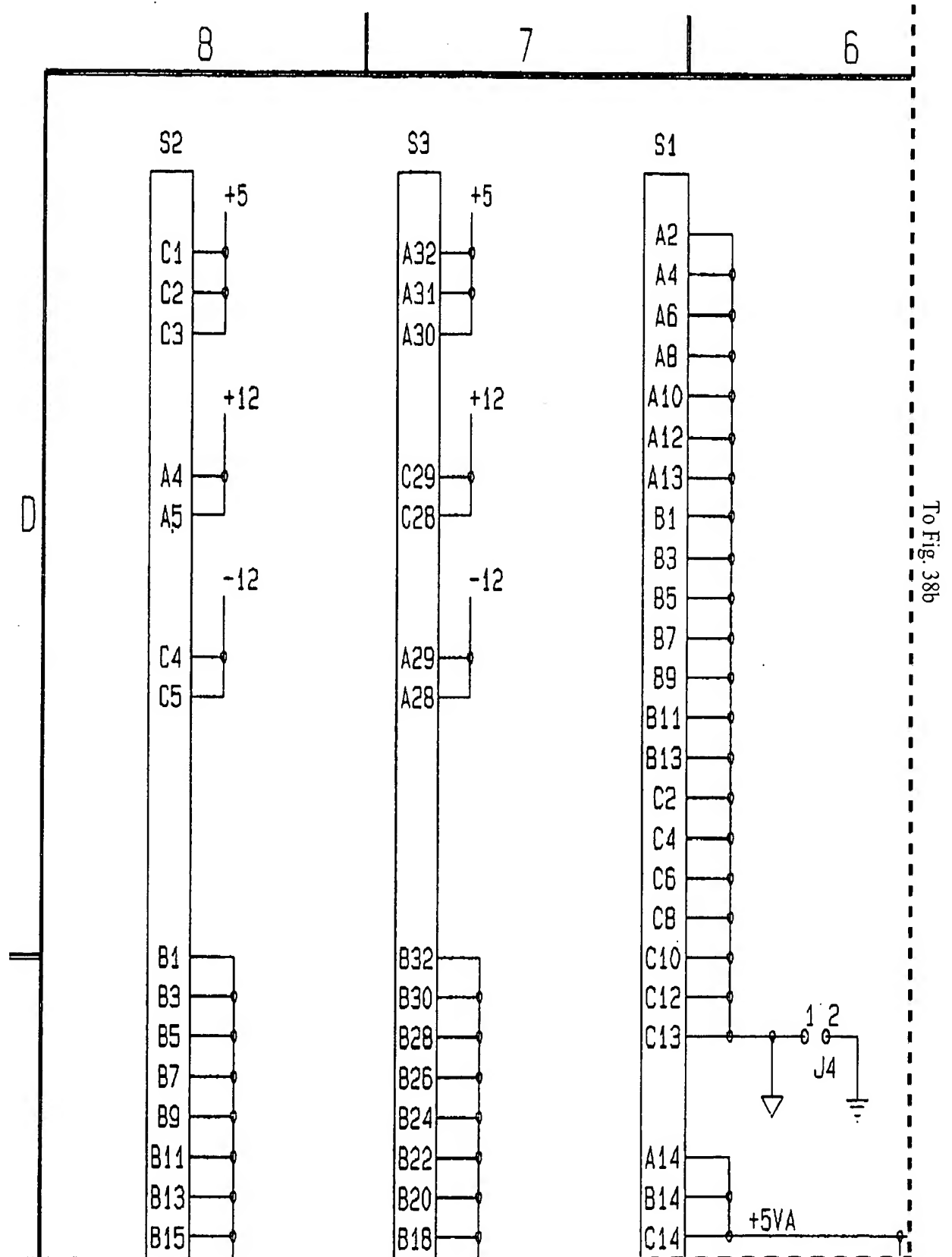
SHEET 7 OF 7

3

2

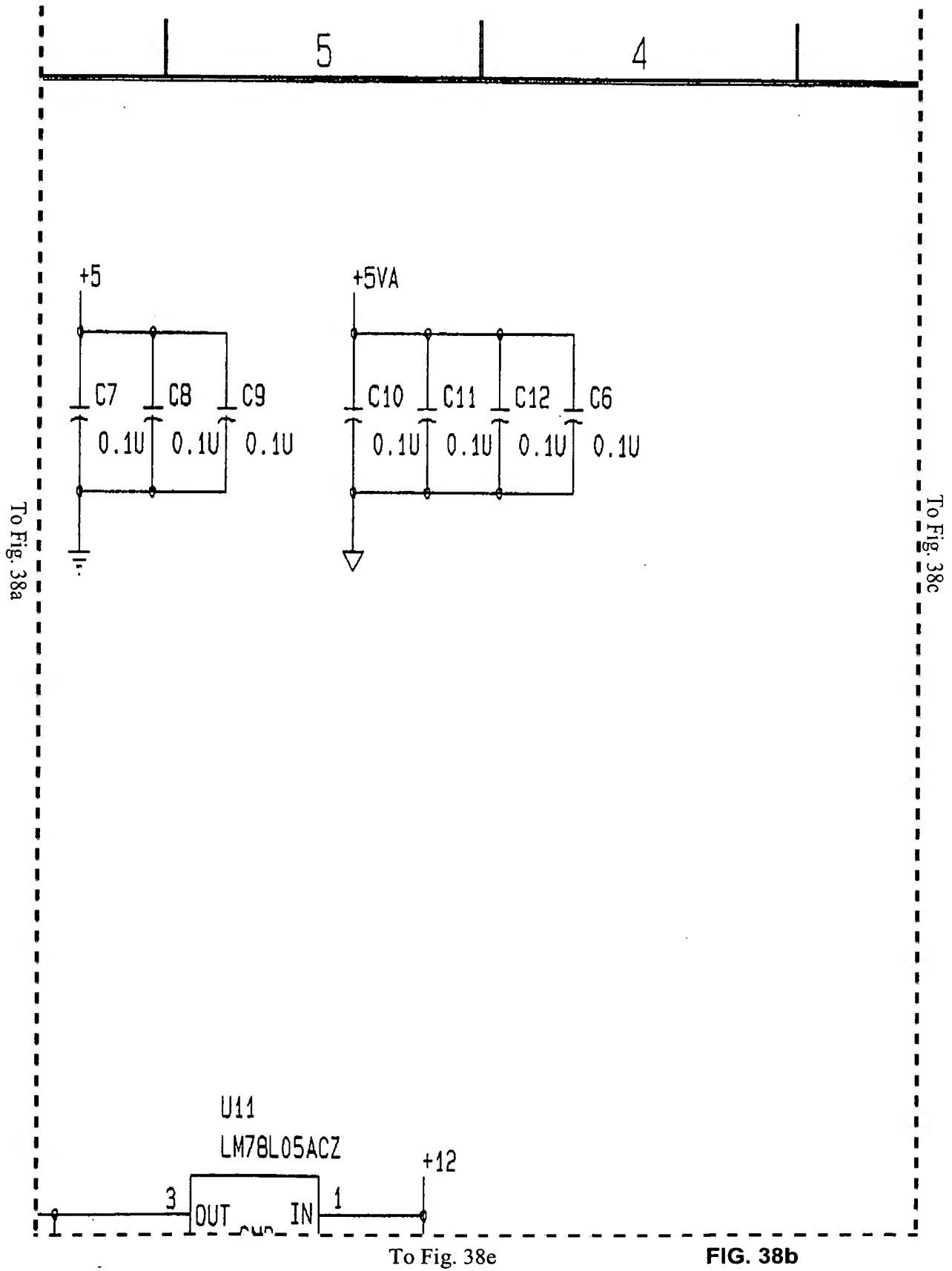
1

FIG. 37i



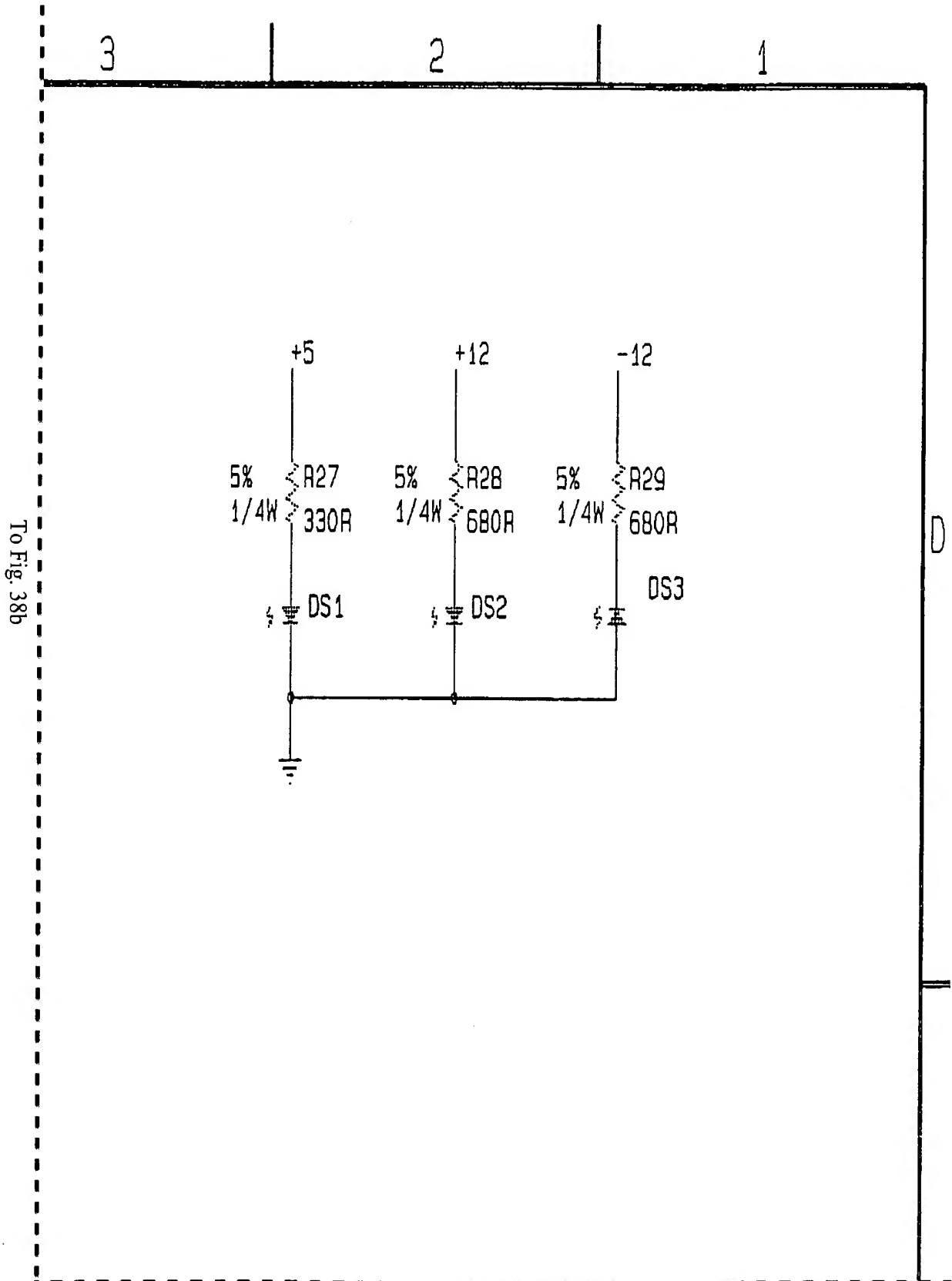
To Fig. 38d

FIG. 38a



To Fig. 38e

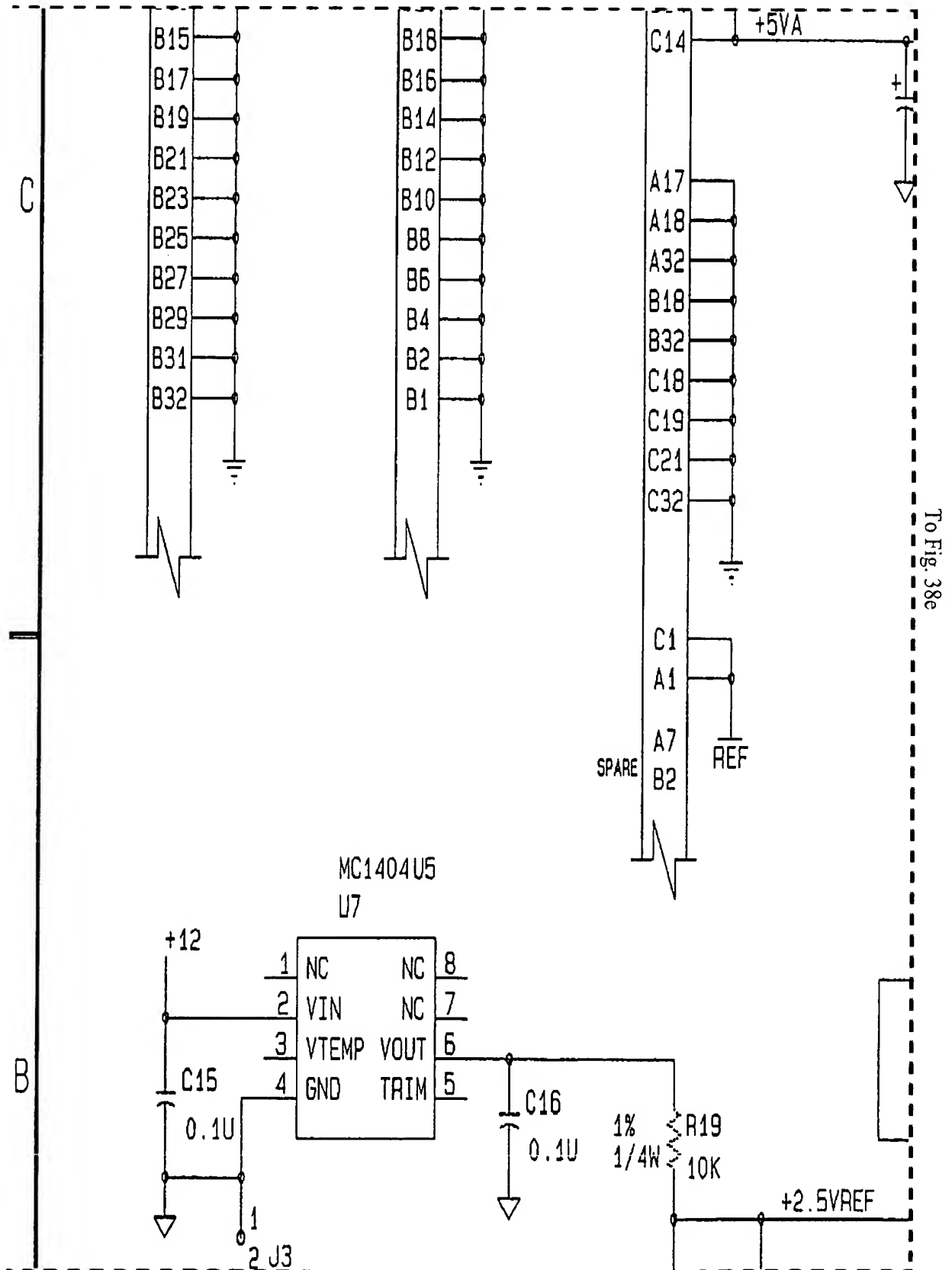
FIG. 38b



To Fig. 38f

FIG. 38c

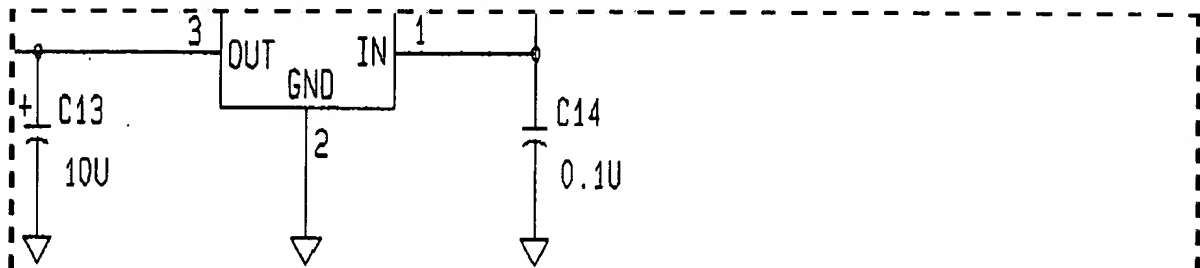
To Fig. 38a



To Fig. 38g

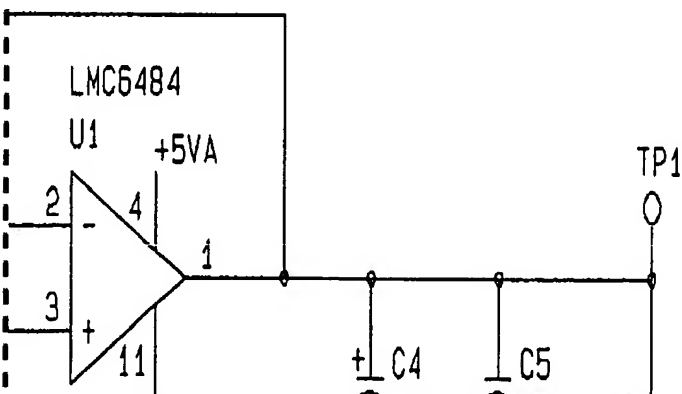
FIG. 38d

To Fig. 38b



To Fig. 38d

To Fig. 38f



To Fig. 38h

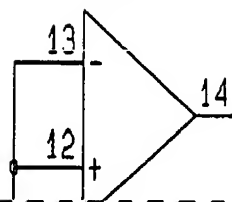
FIG. 38e

To Fig. 38c

To Fig. 38e

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U10



To Fig. 38i

FIG. 38f

C

B

To Fig. 38d

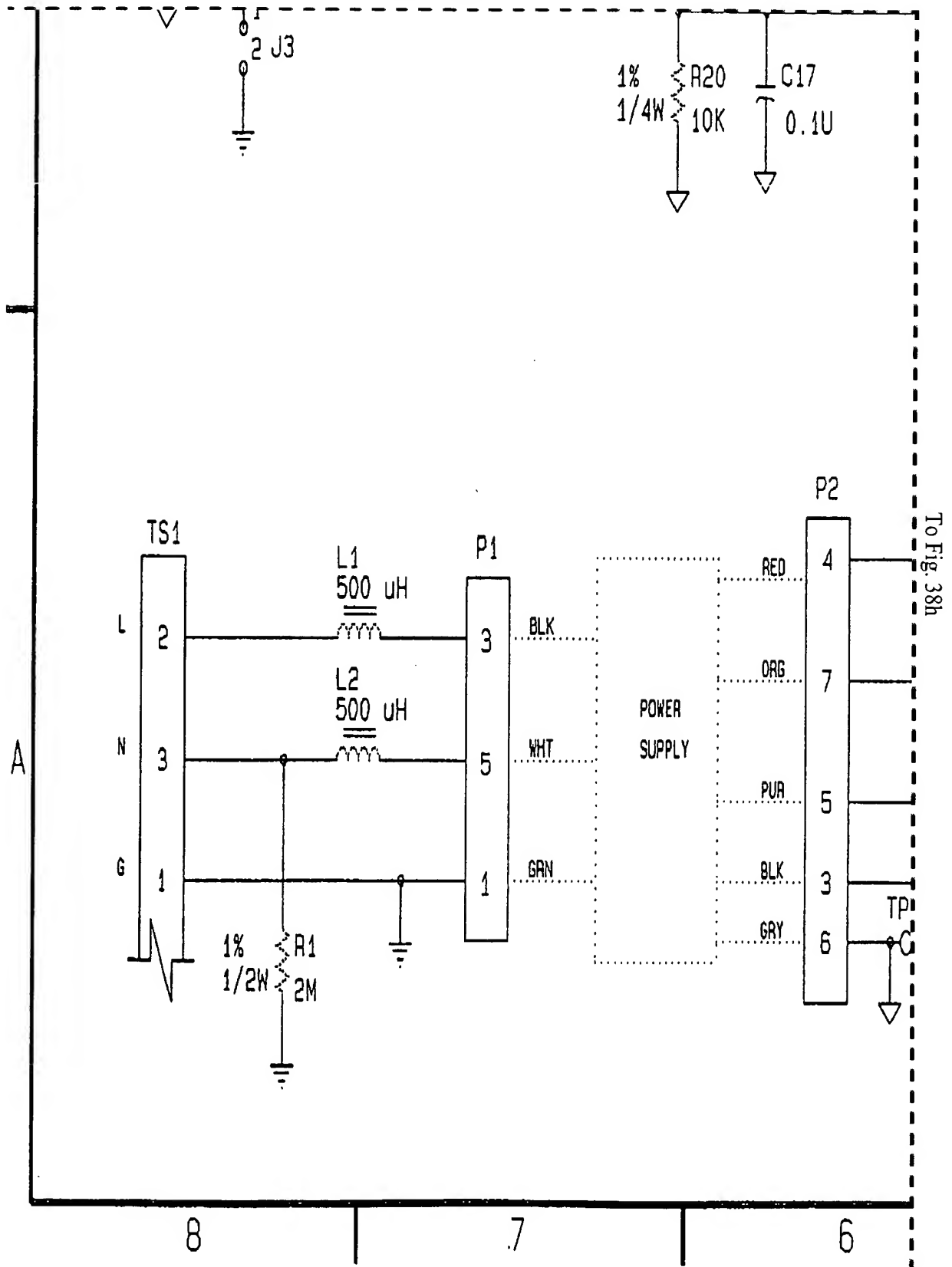


FIG. 38g

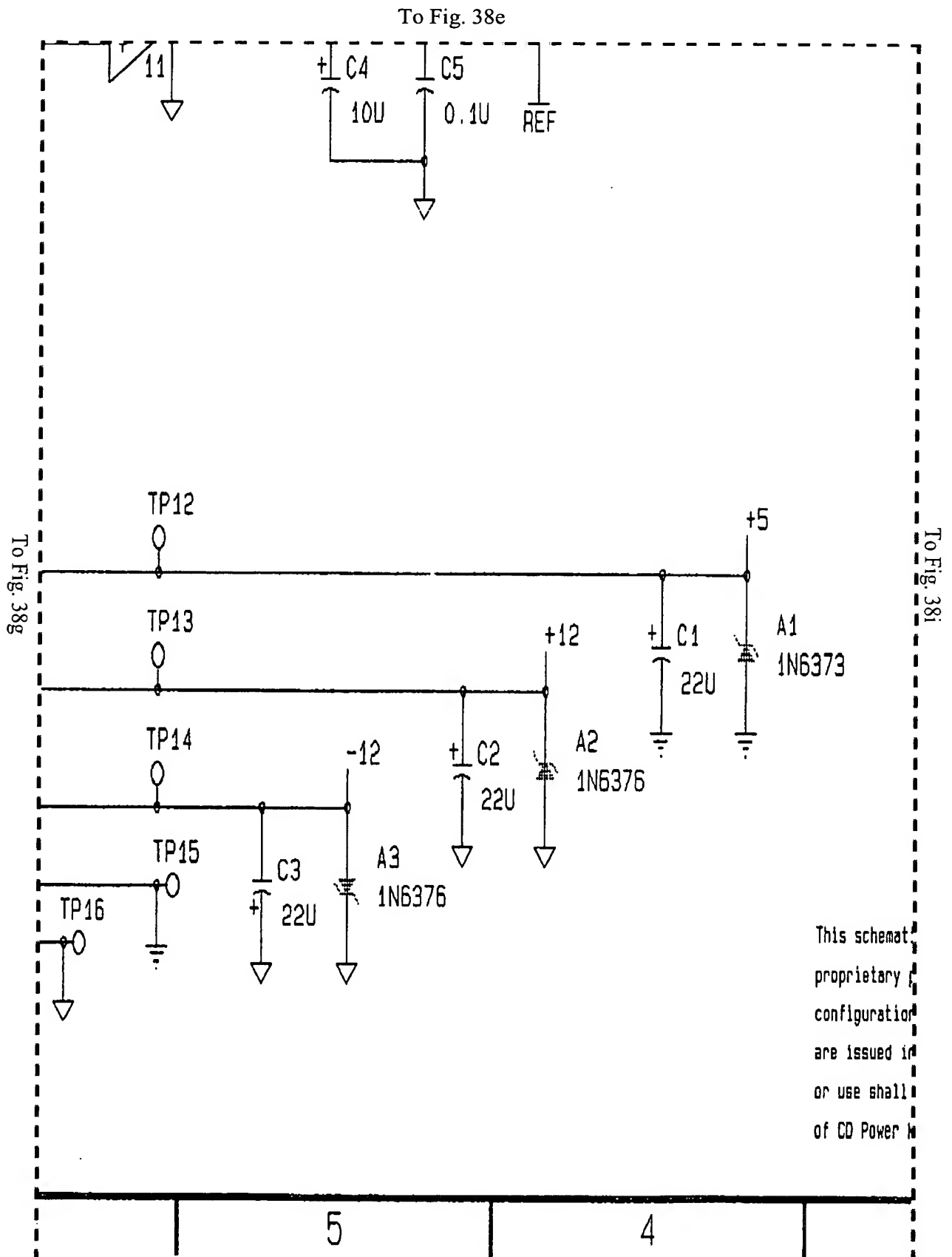
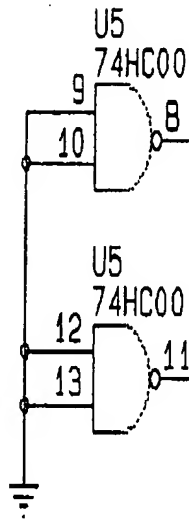
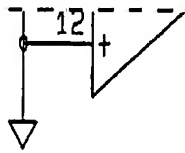


FIG. 38h

To Fig. 38f



LAST USED: U11
R39
C30
S6
P4
A16
DS3
TP16
J5
PTC3
TS3
L2
T4

To Fig. 38h

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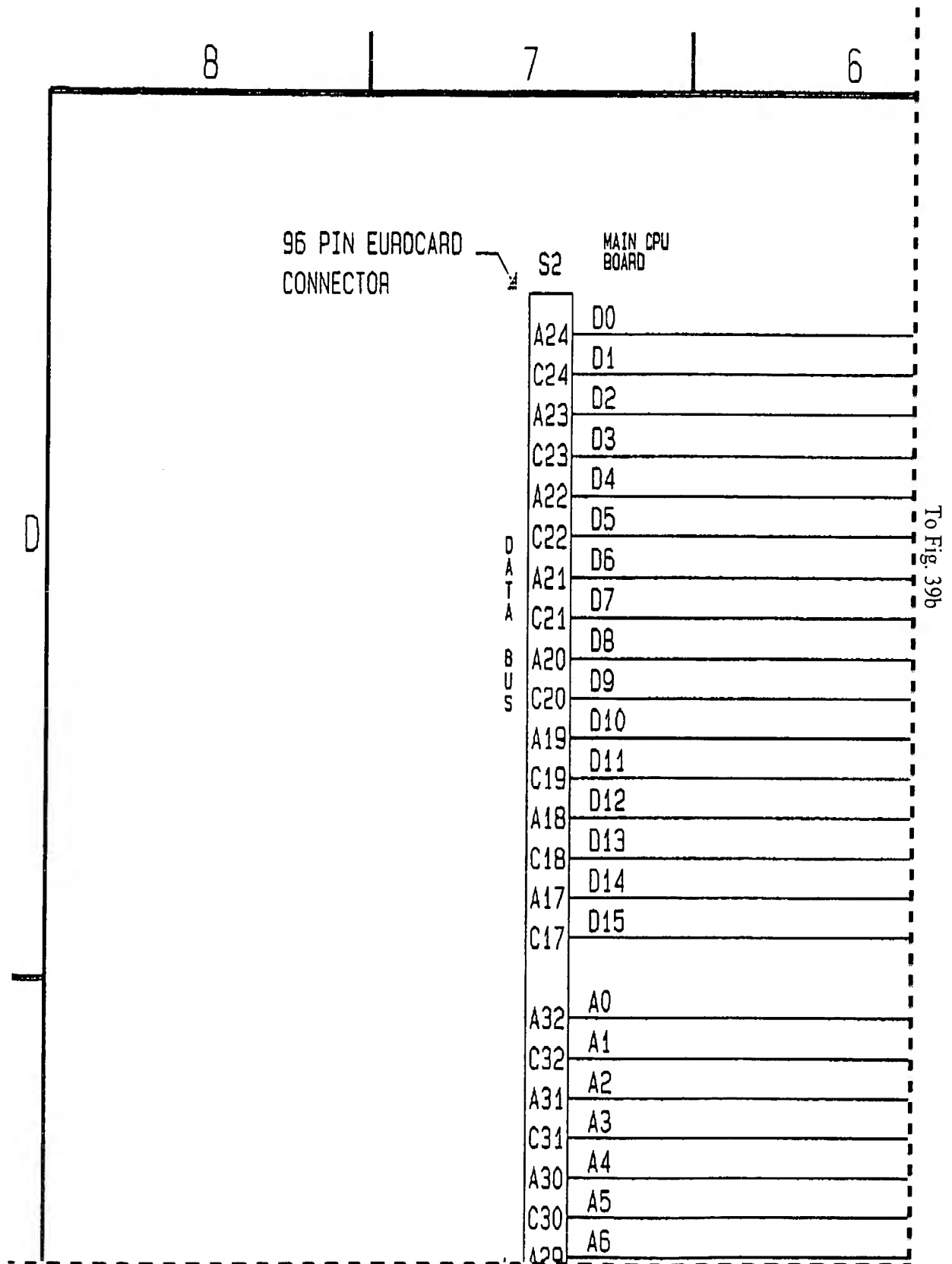
SHEET 1 OF 7

3

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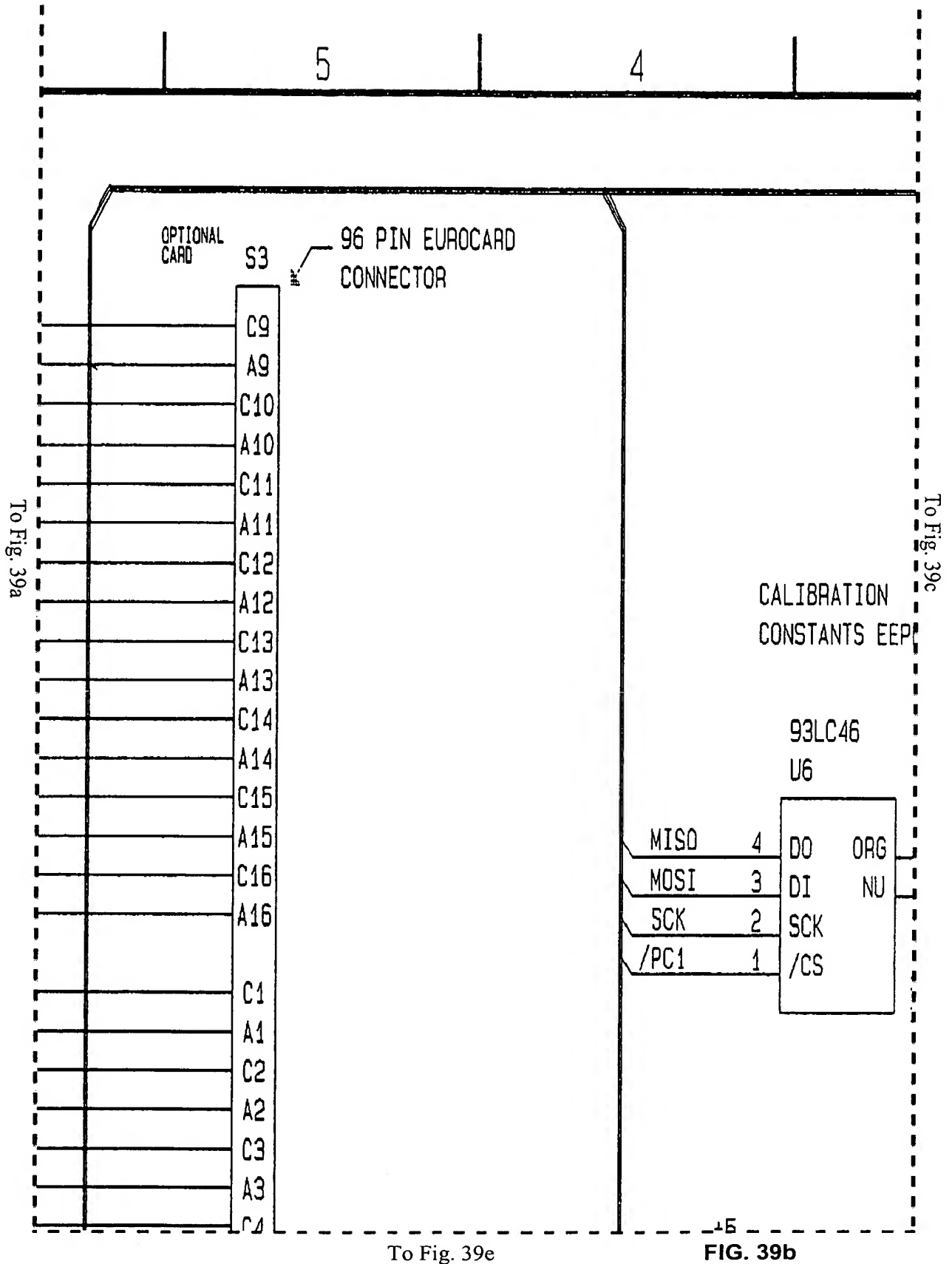
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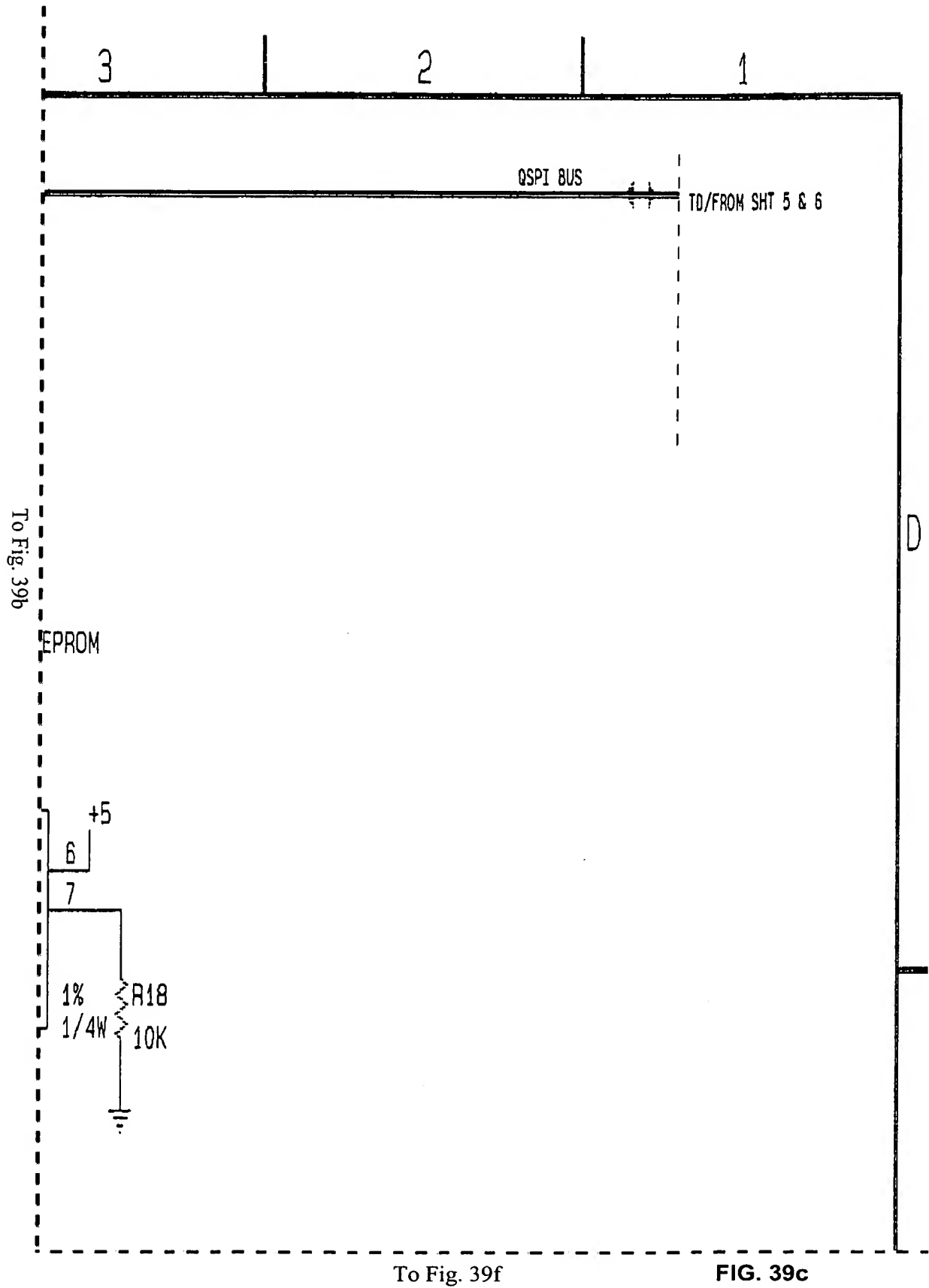
FIG. 38i



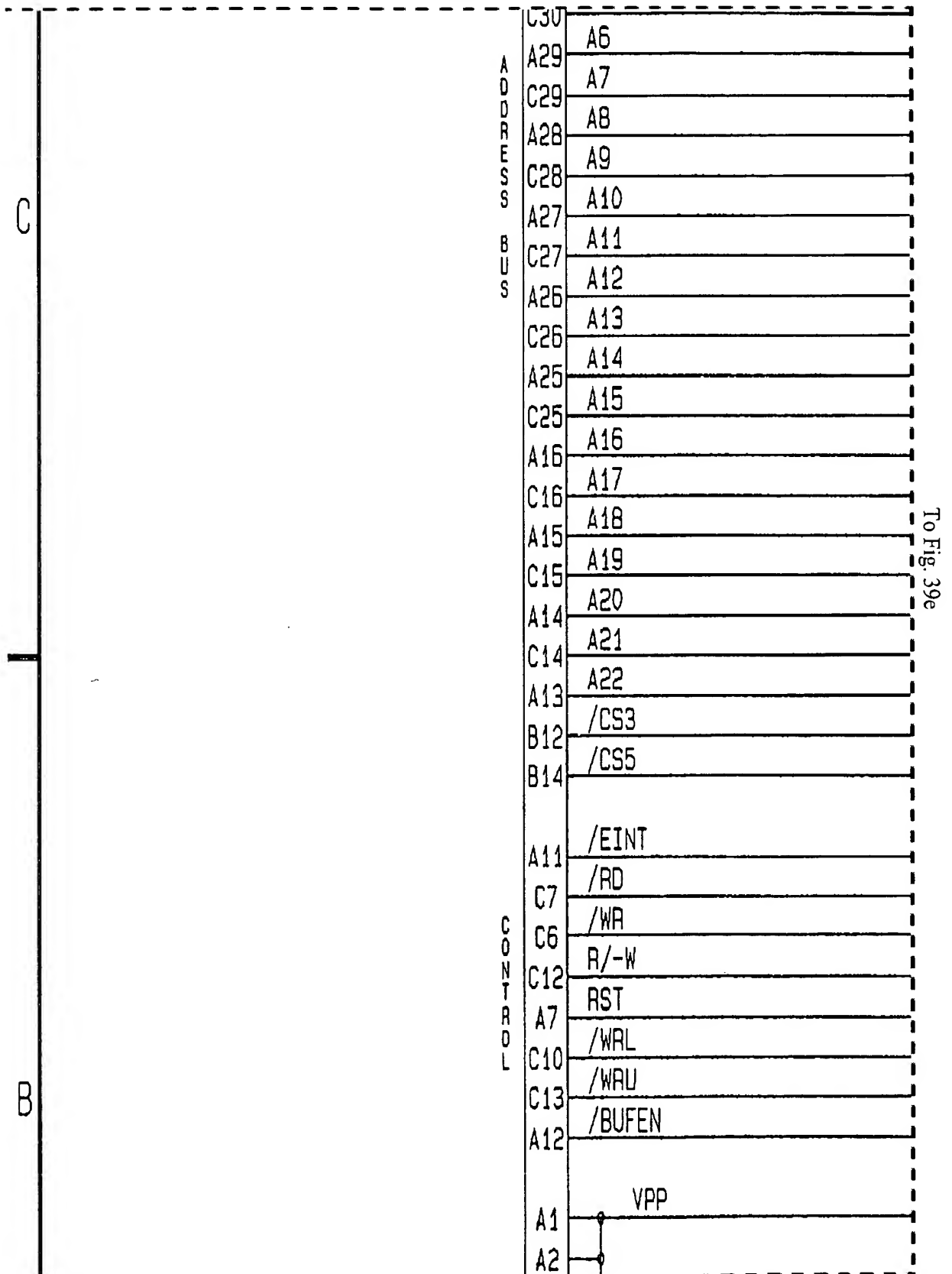
To Fig. 39d

FIG. 39a





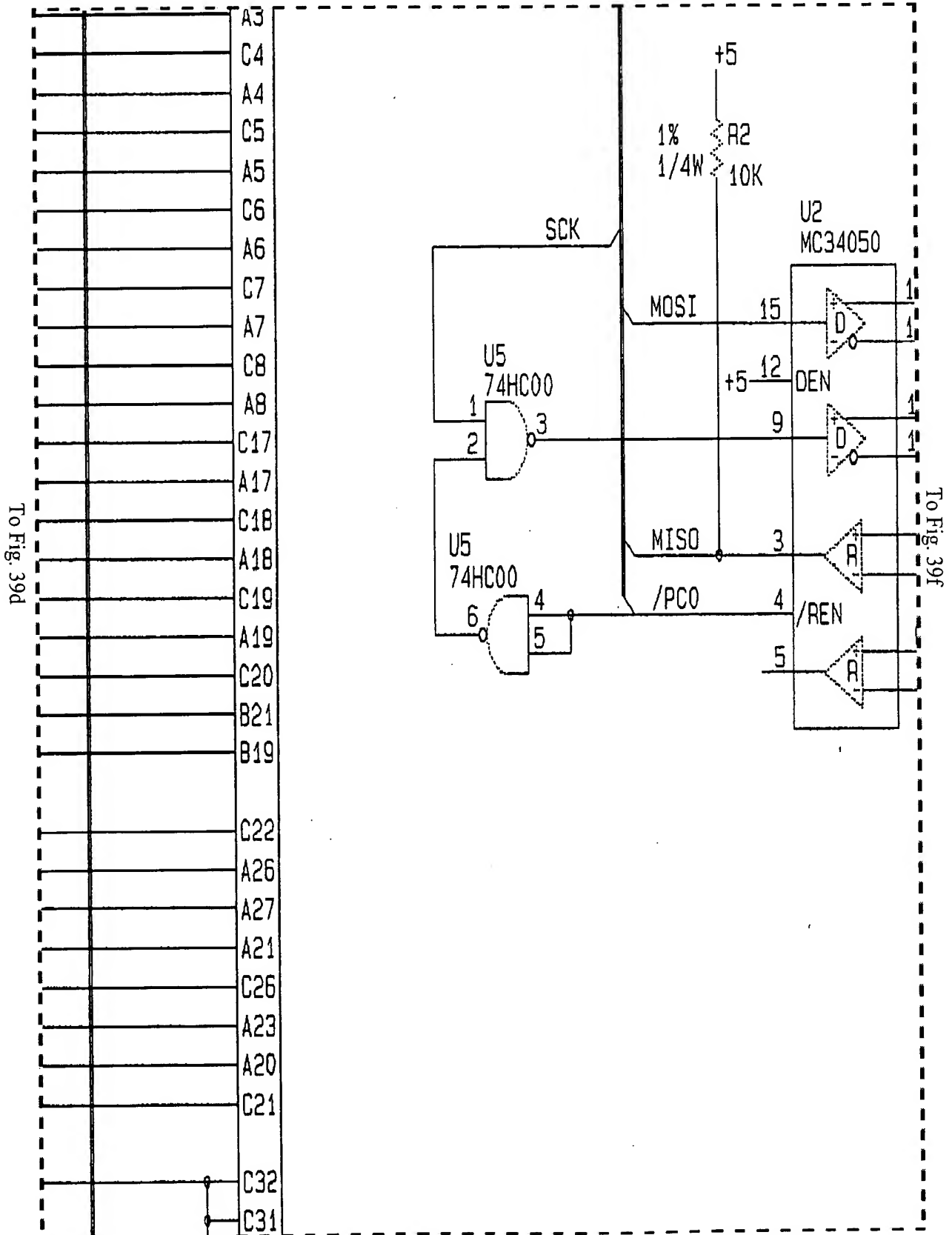
To Fig. 39a



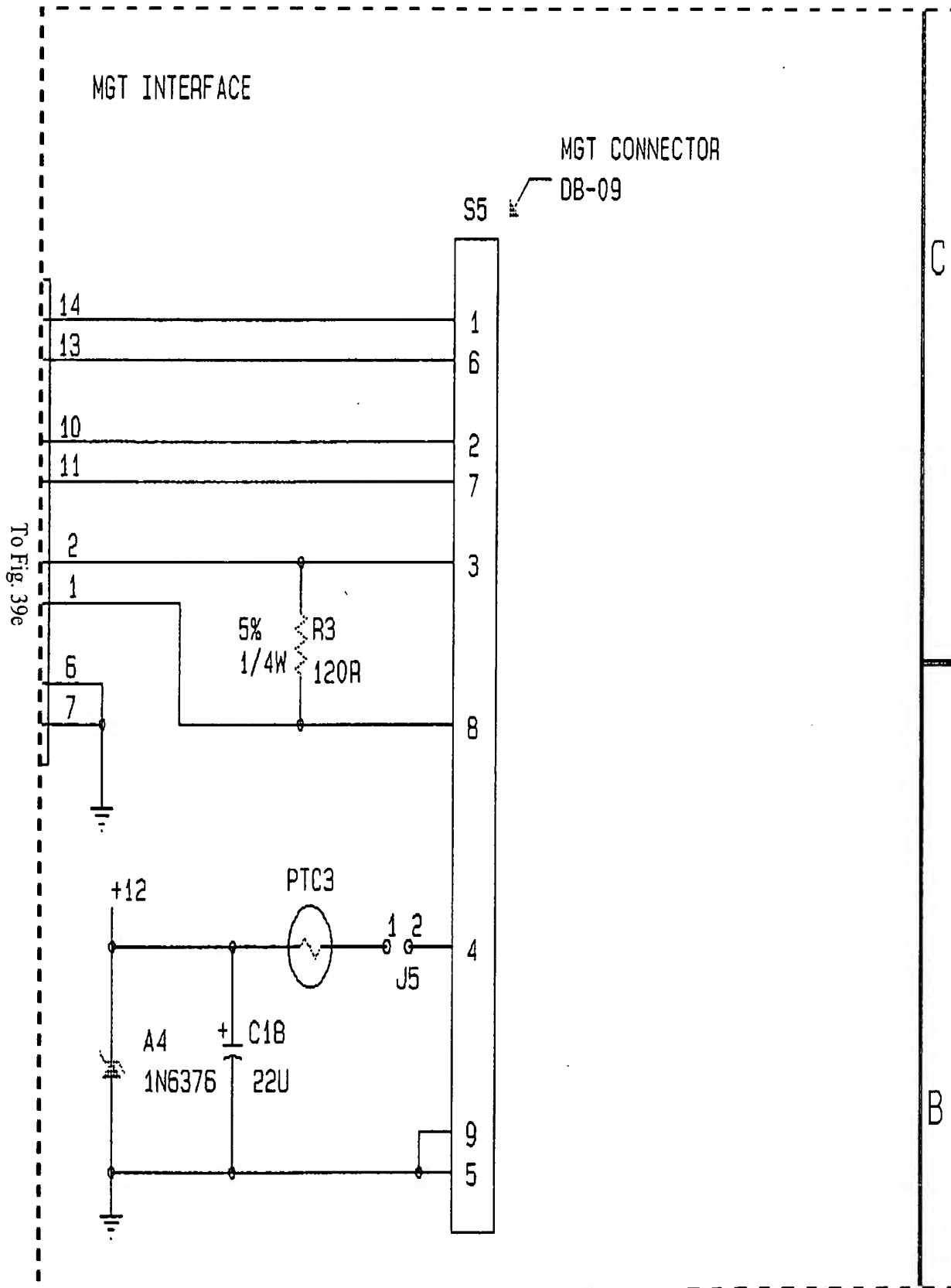
To Fig. 39g

FIG. 39d

To Fig. 39b



To Fig. 39c



To Fig. 39i

FIG. 39f

To Fig. 39d

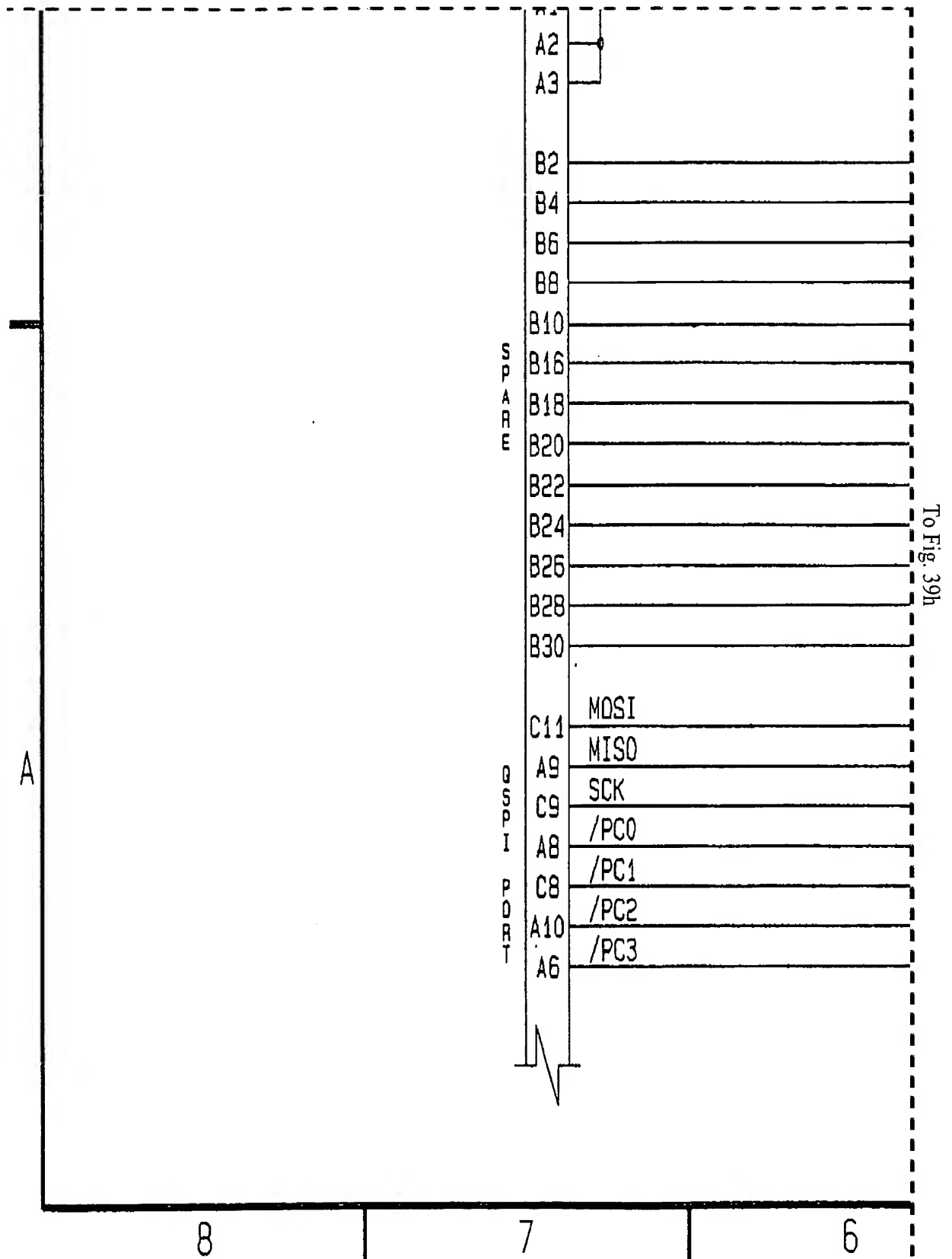
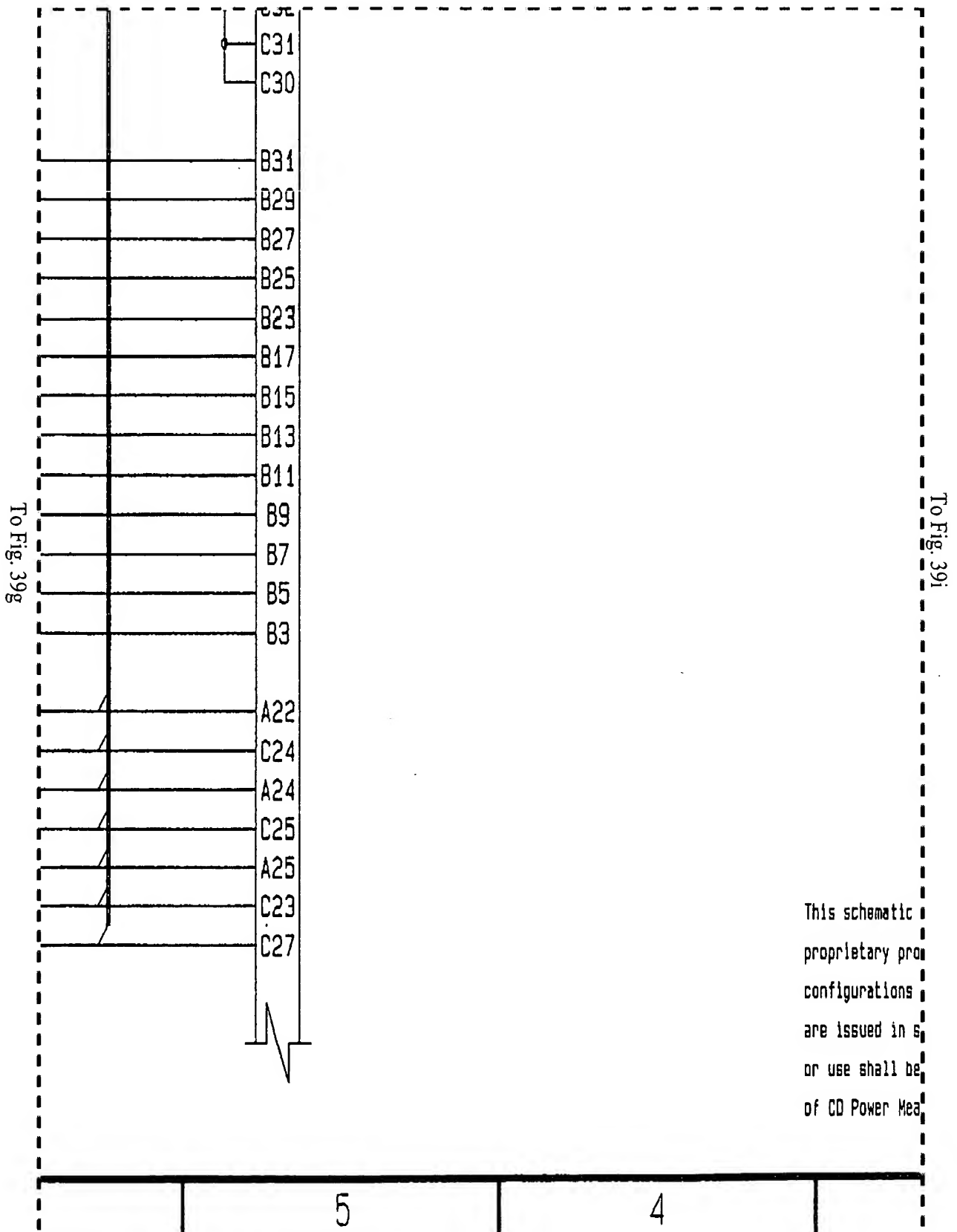


FIG. 39g

To Fig. 39e



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FIG. 39h

To Fig. 39f

To Fig. 39h

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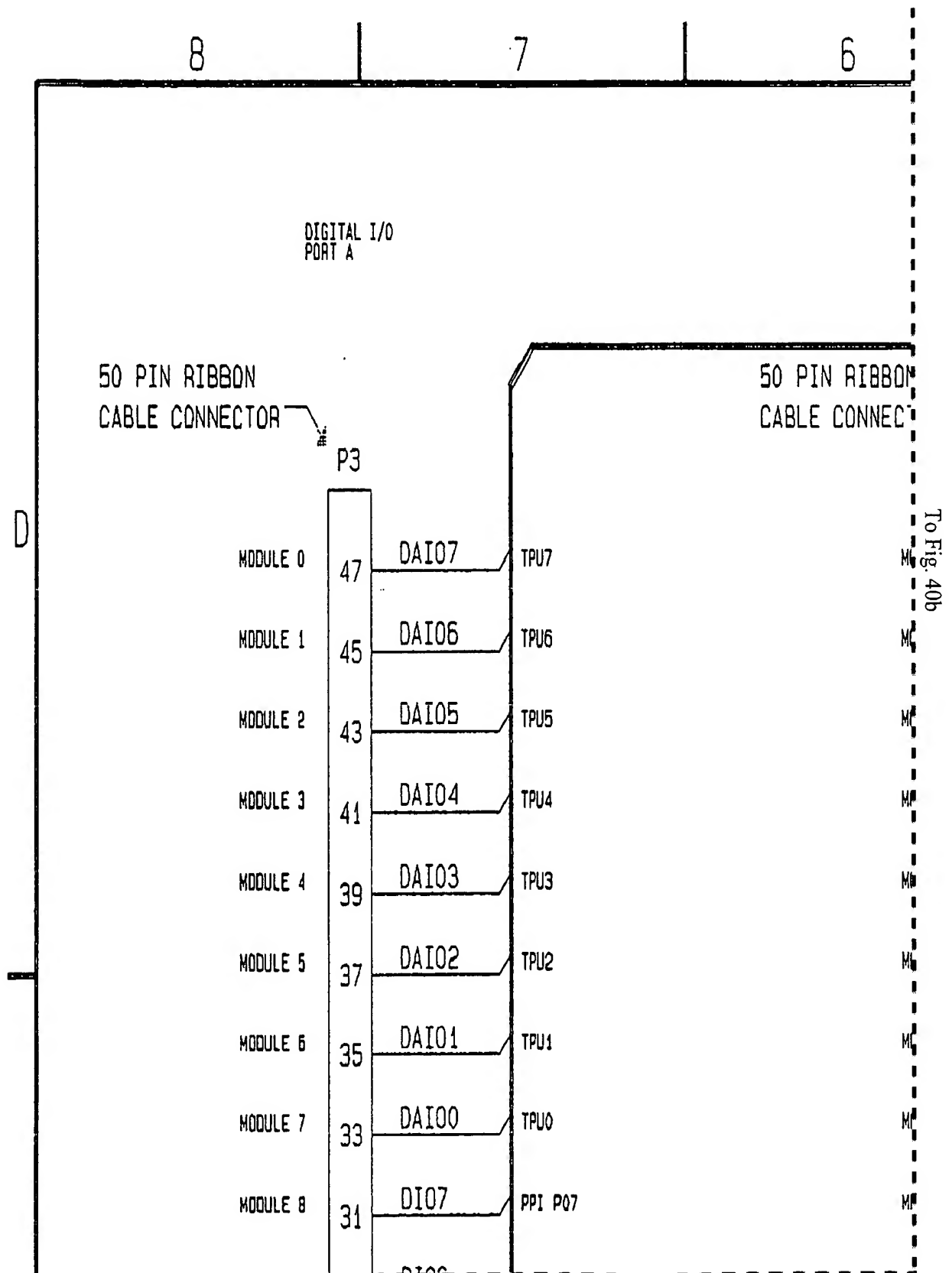
SHEET 2 OF 7

3

2

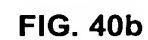
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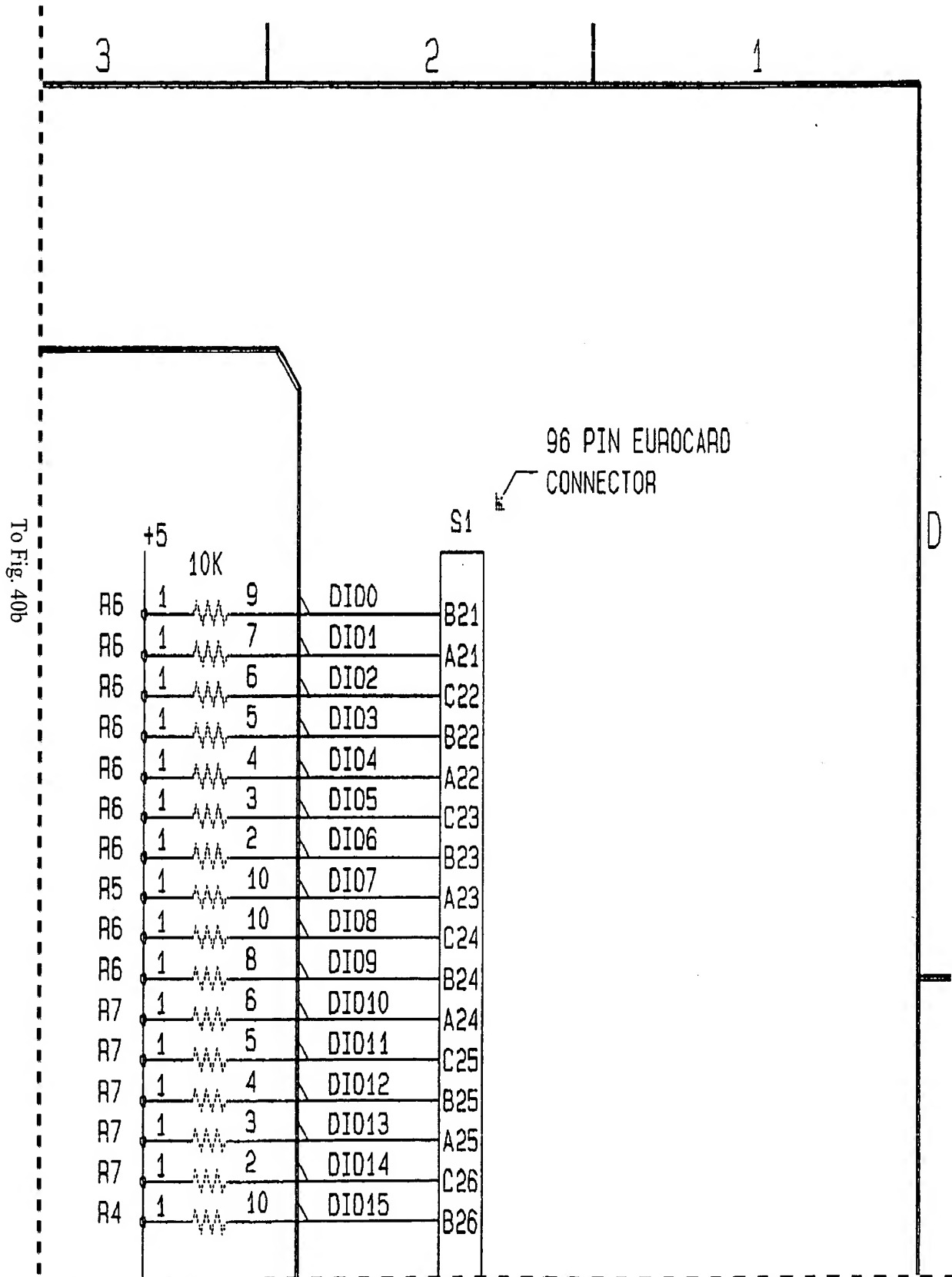
FIG. 39i

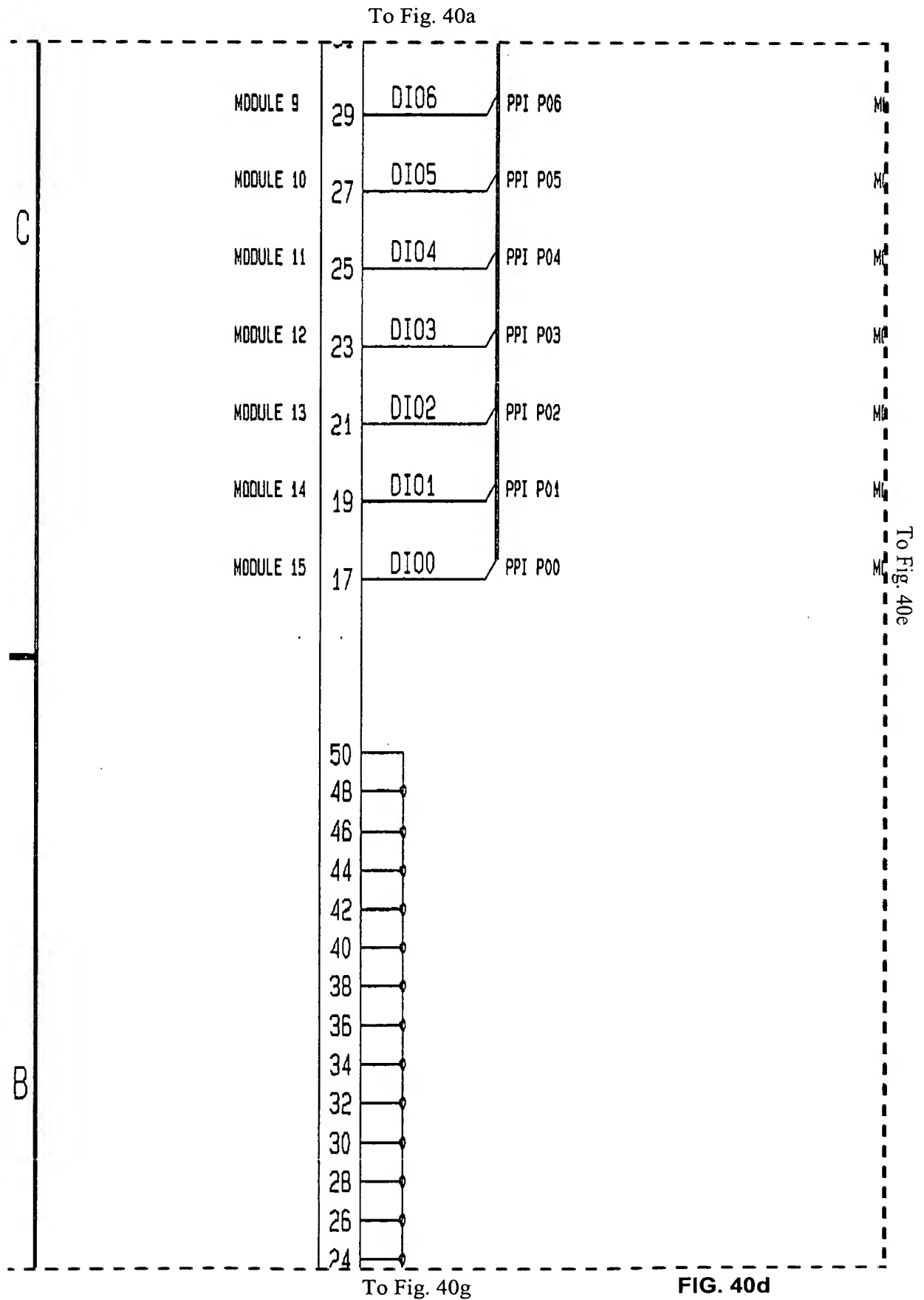


To Fig. 40d

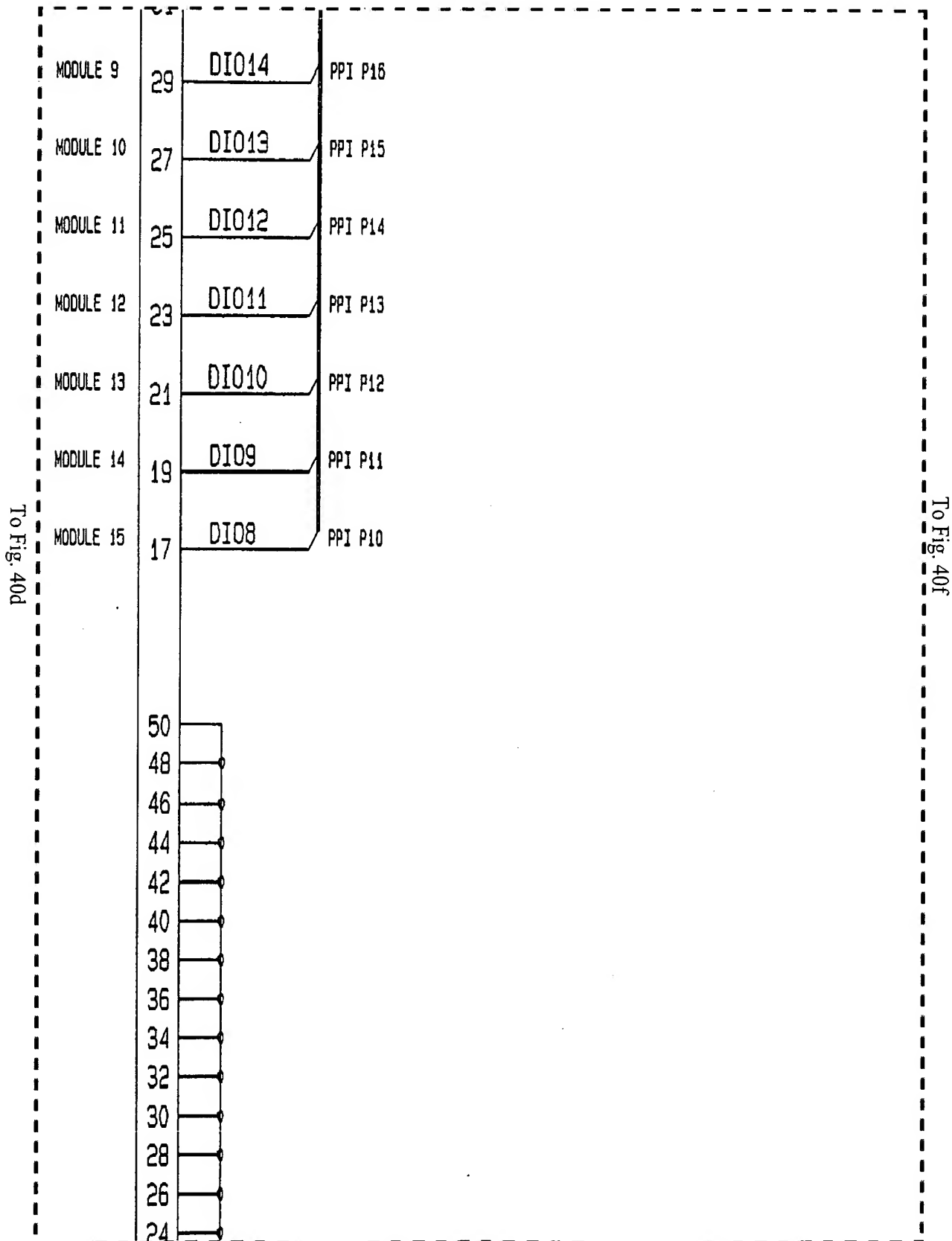
FIG. 40a







To Fig. 40b

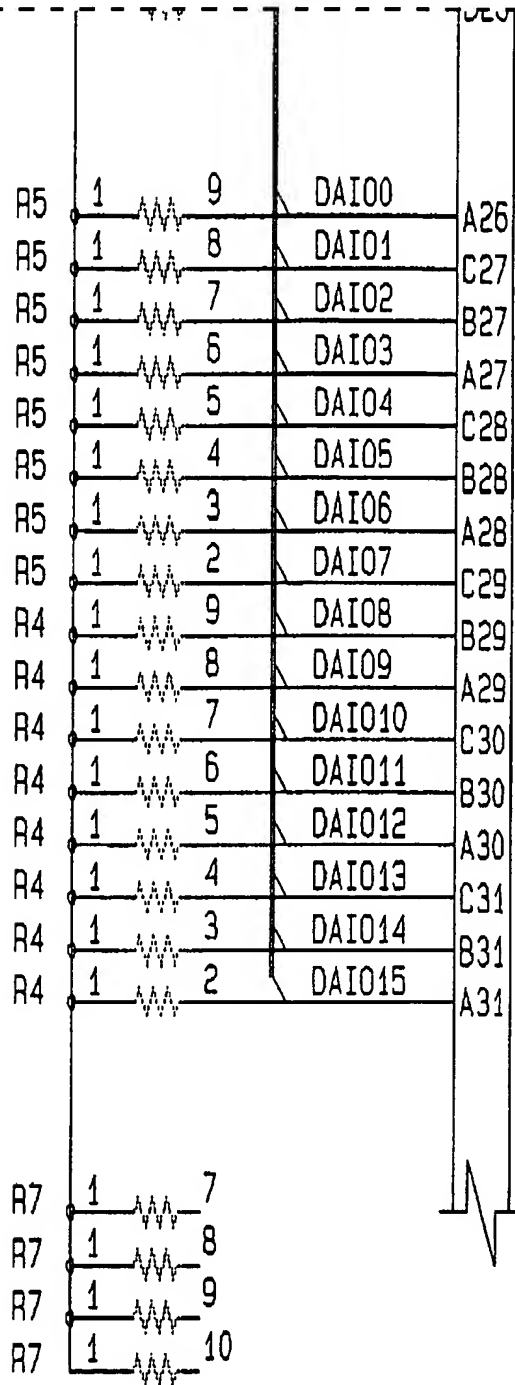


To Fig. 40h

FIG. 40e

To Fig. 40c

To Fig. 40e



To Fig. 40i

FIG. 40f

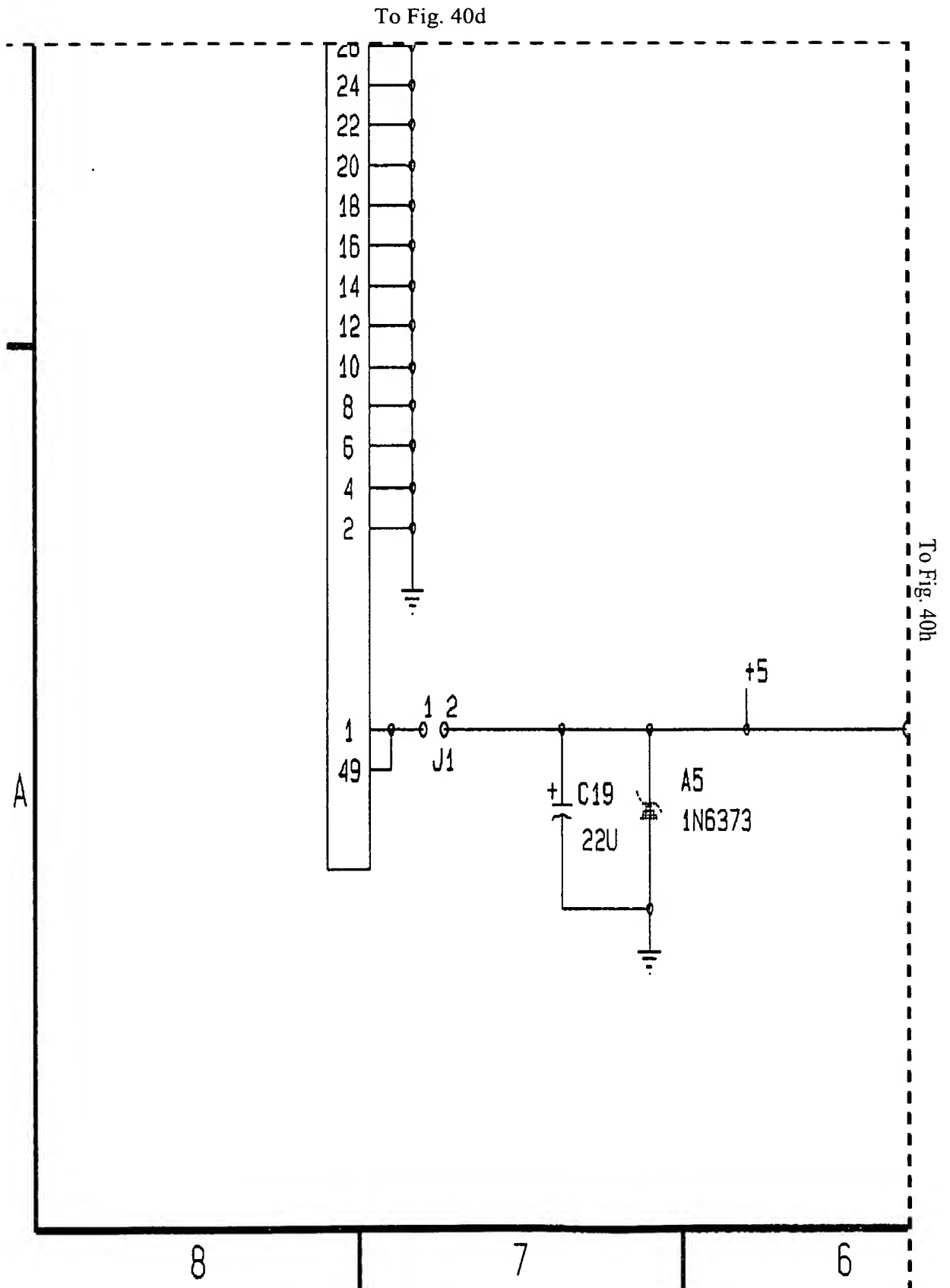
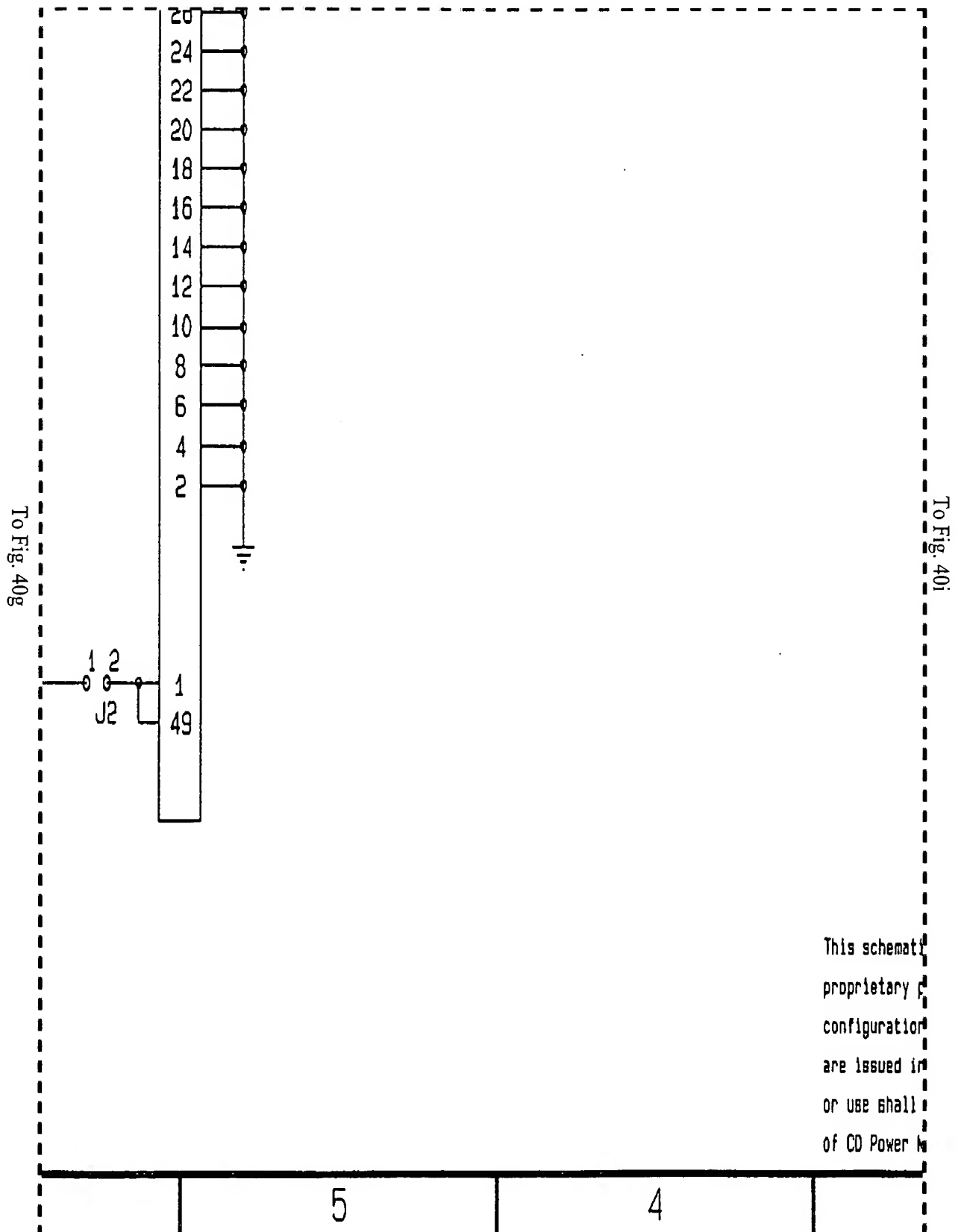


FIG. 40g

To Fig. 40e

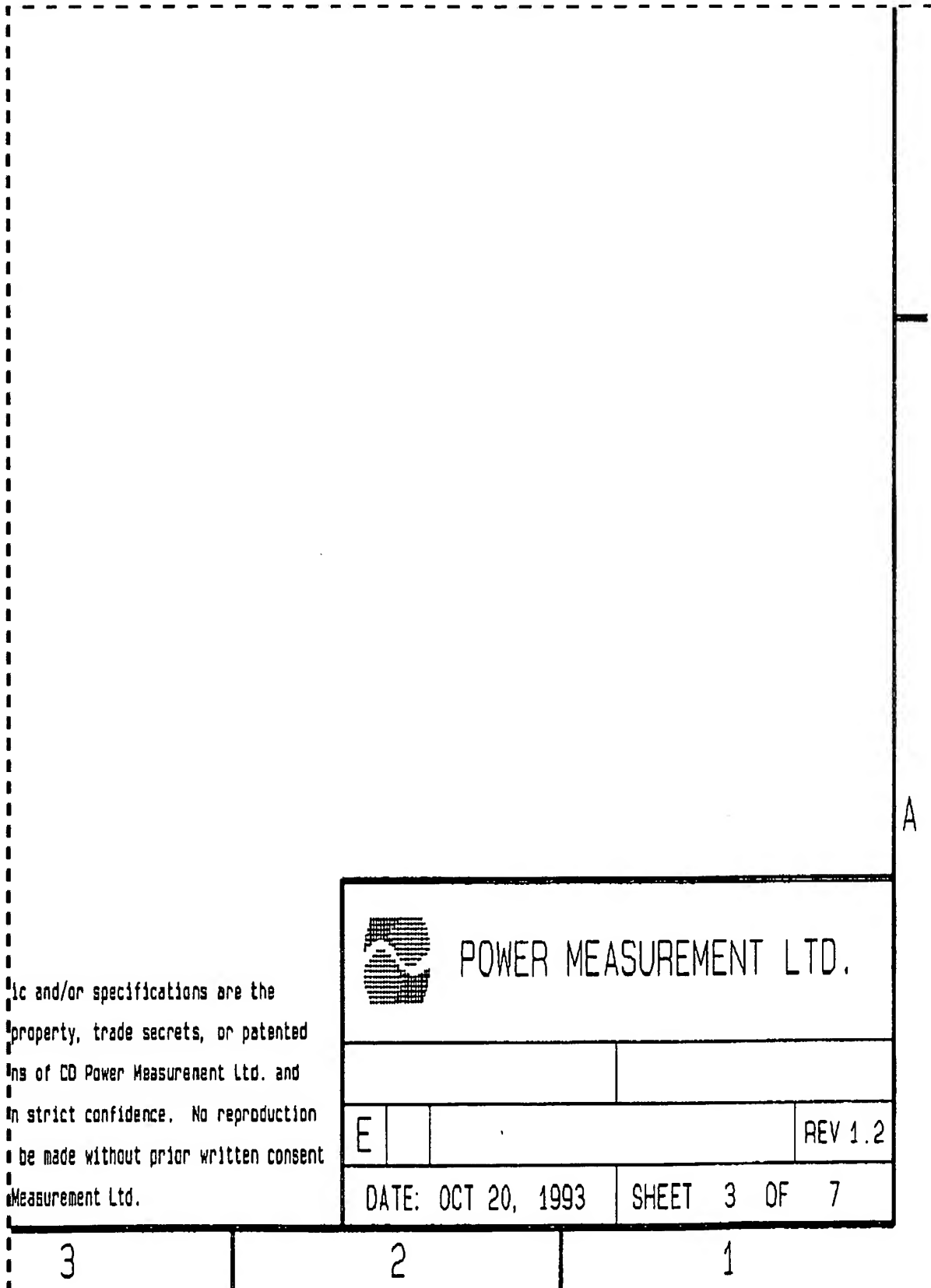


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FIG. 40h

To Fig. 40f

To Fig. 40h



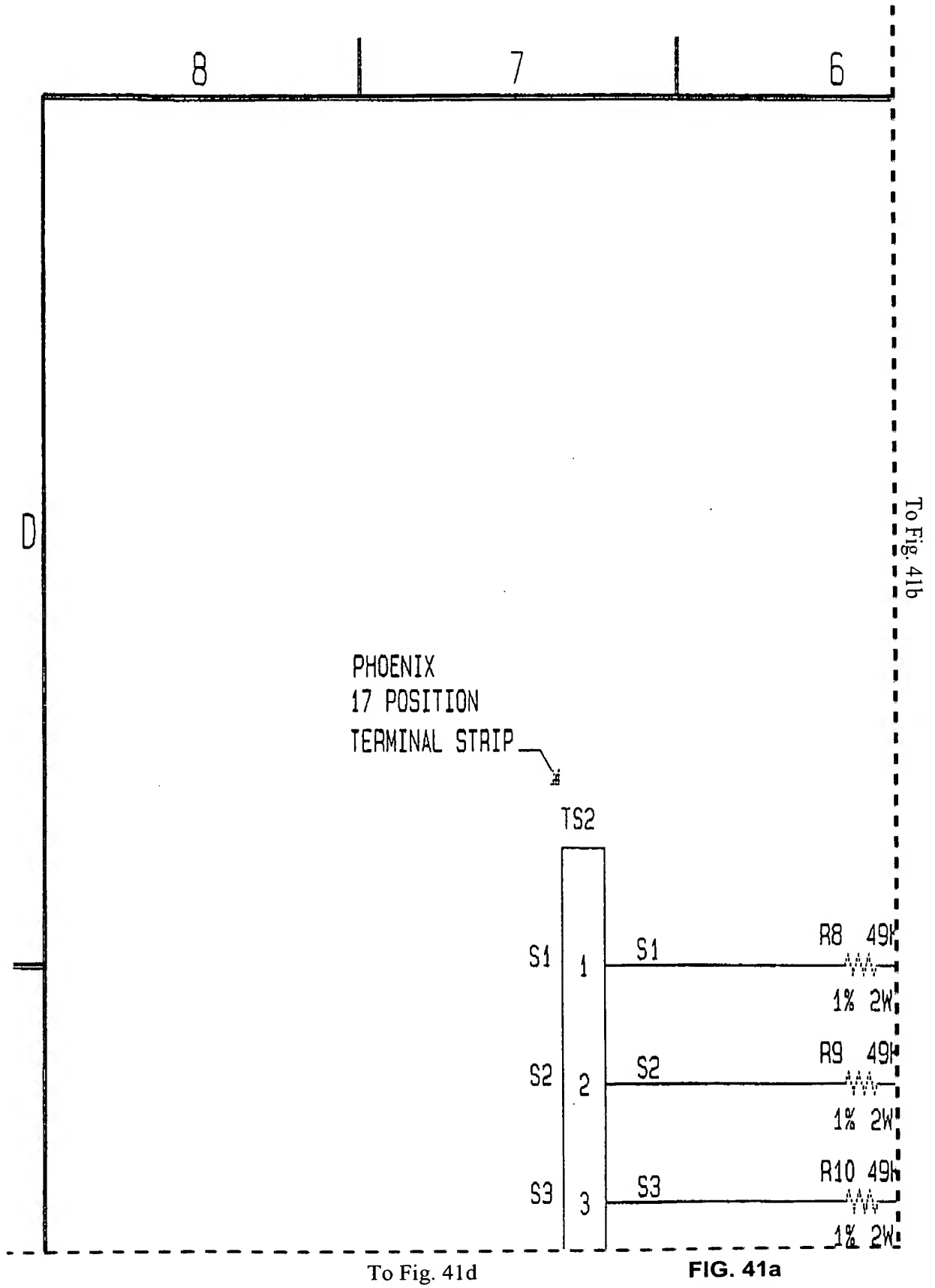
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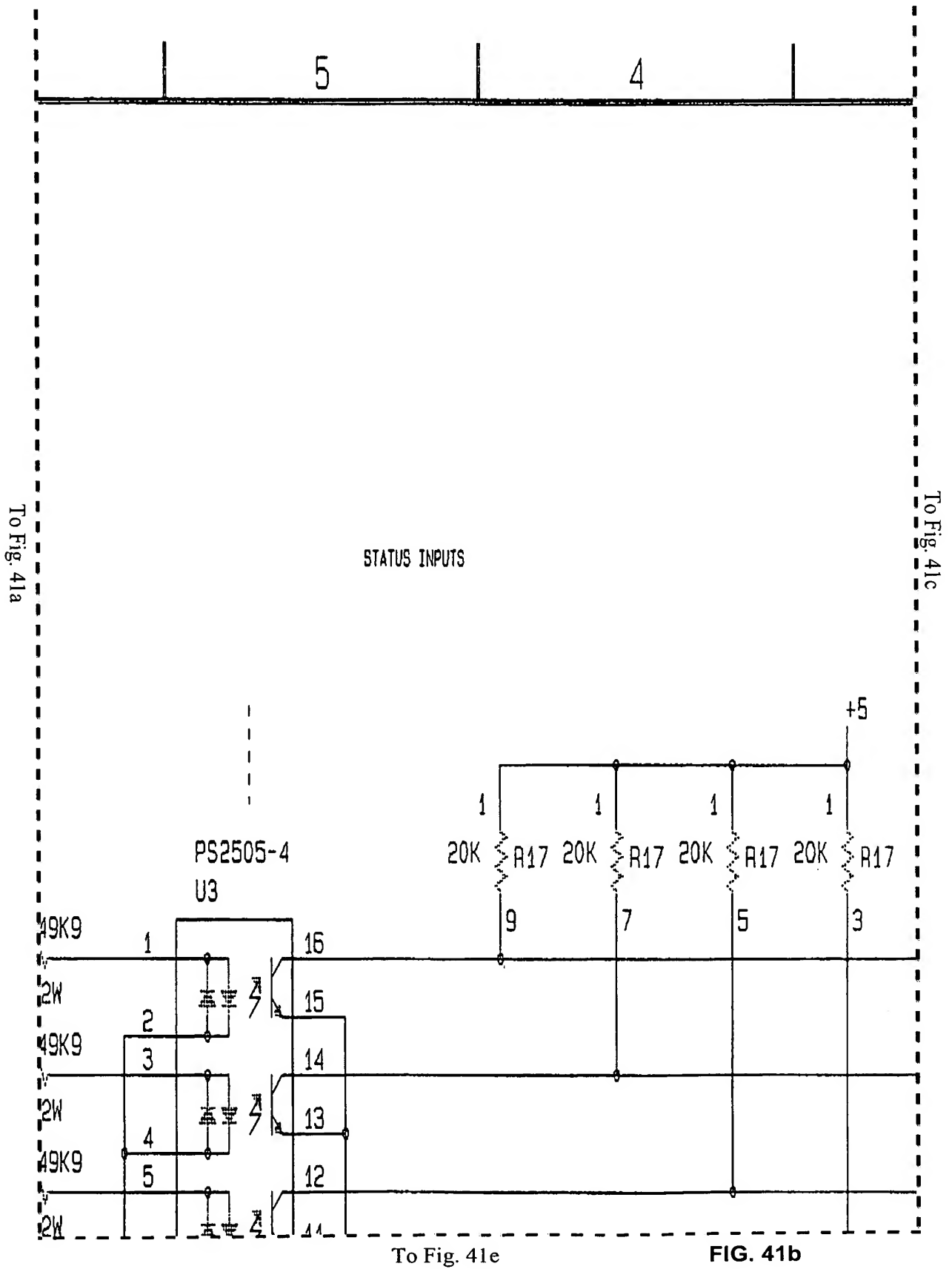
3

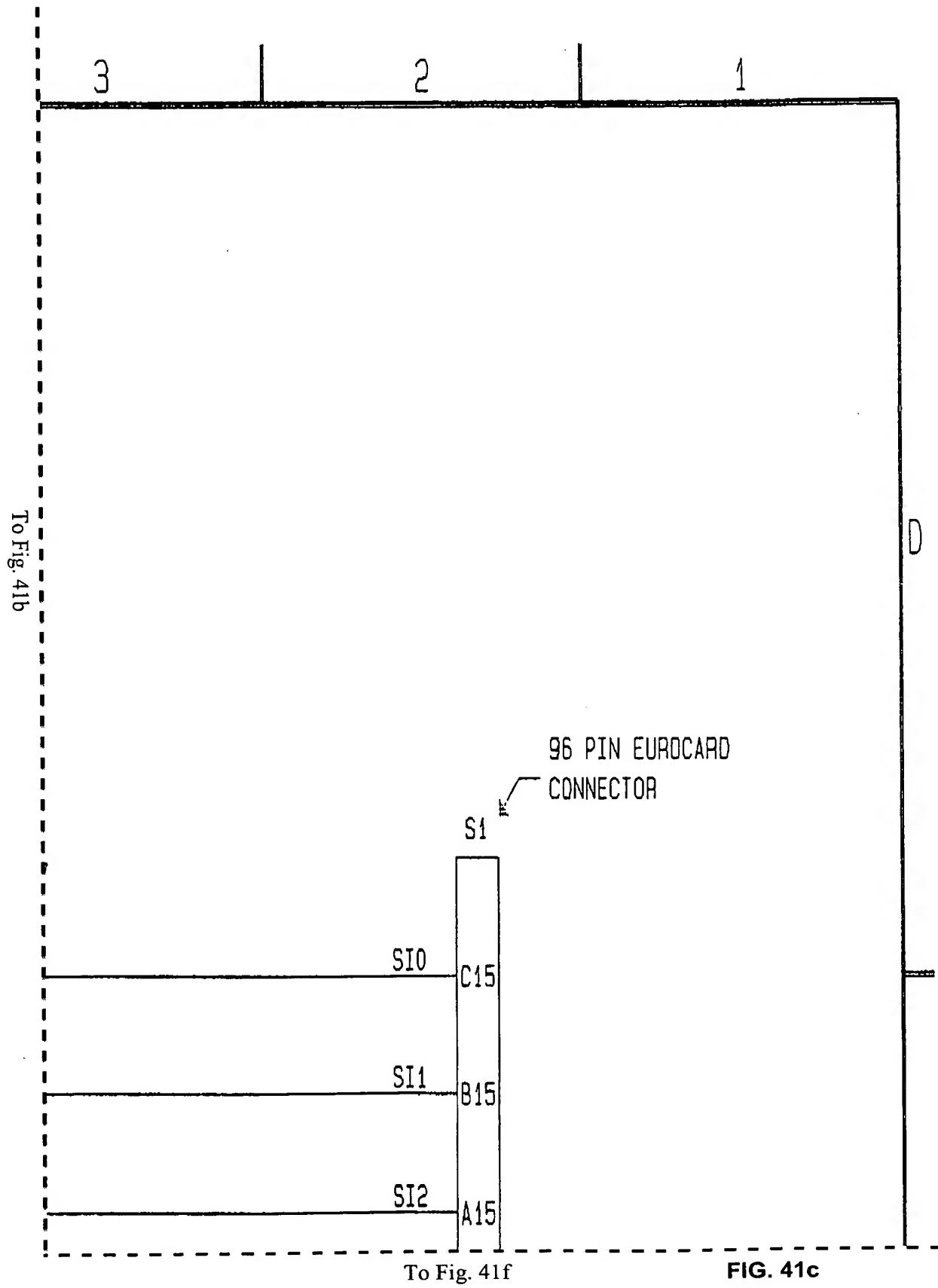
2

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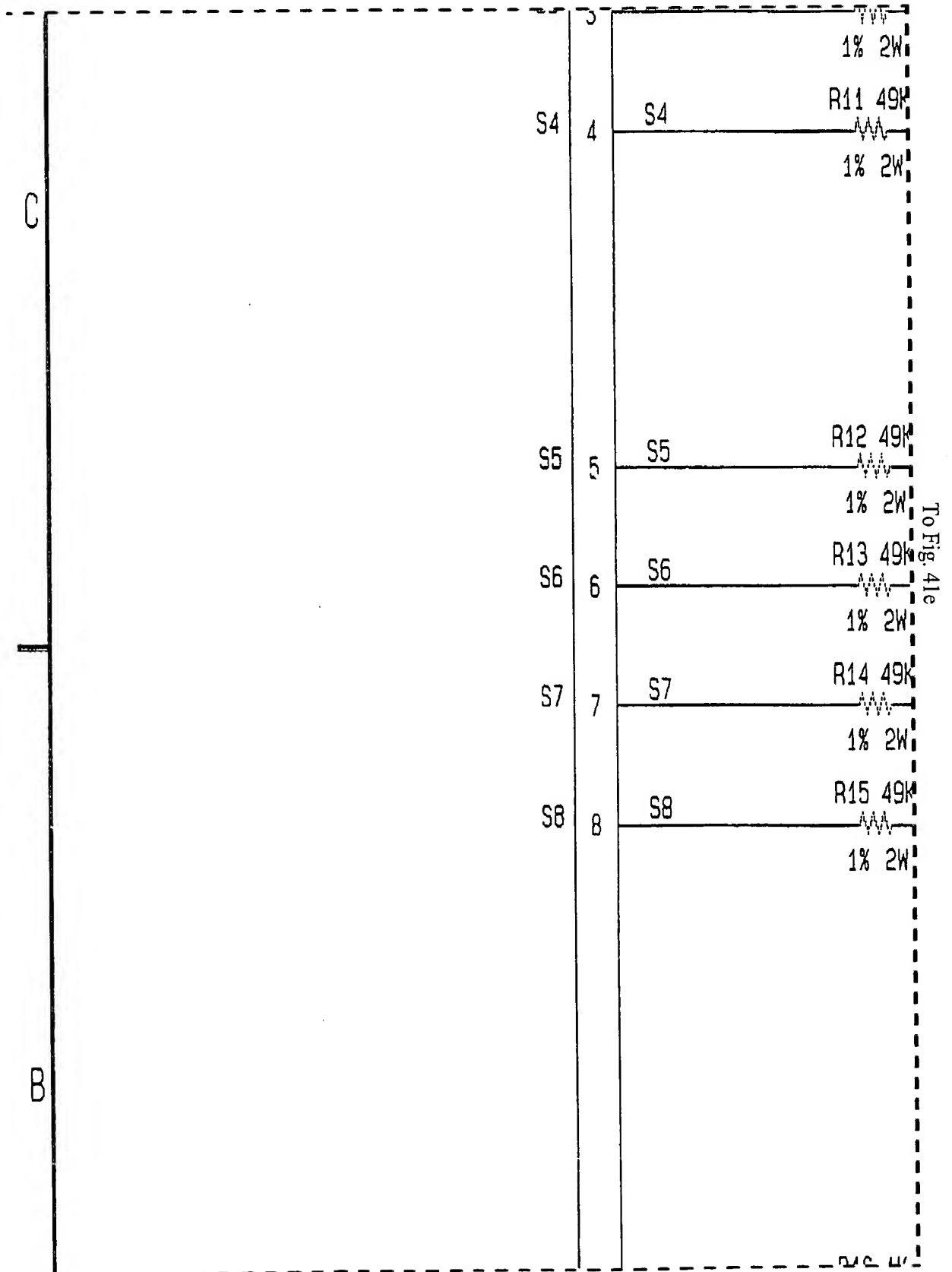
FIG. 40i







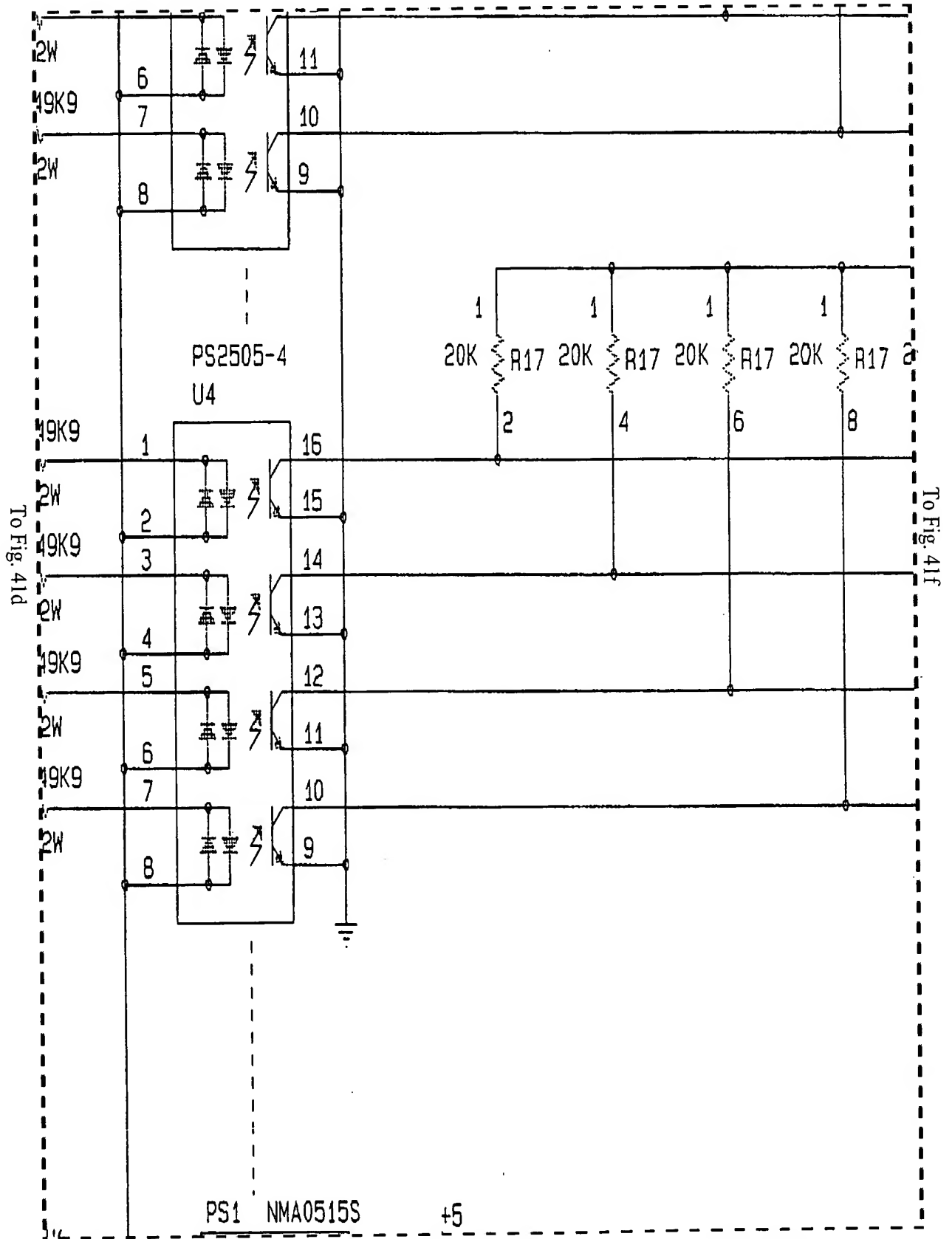
To Fig. 41a



To Fig. 41g

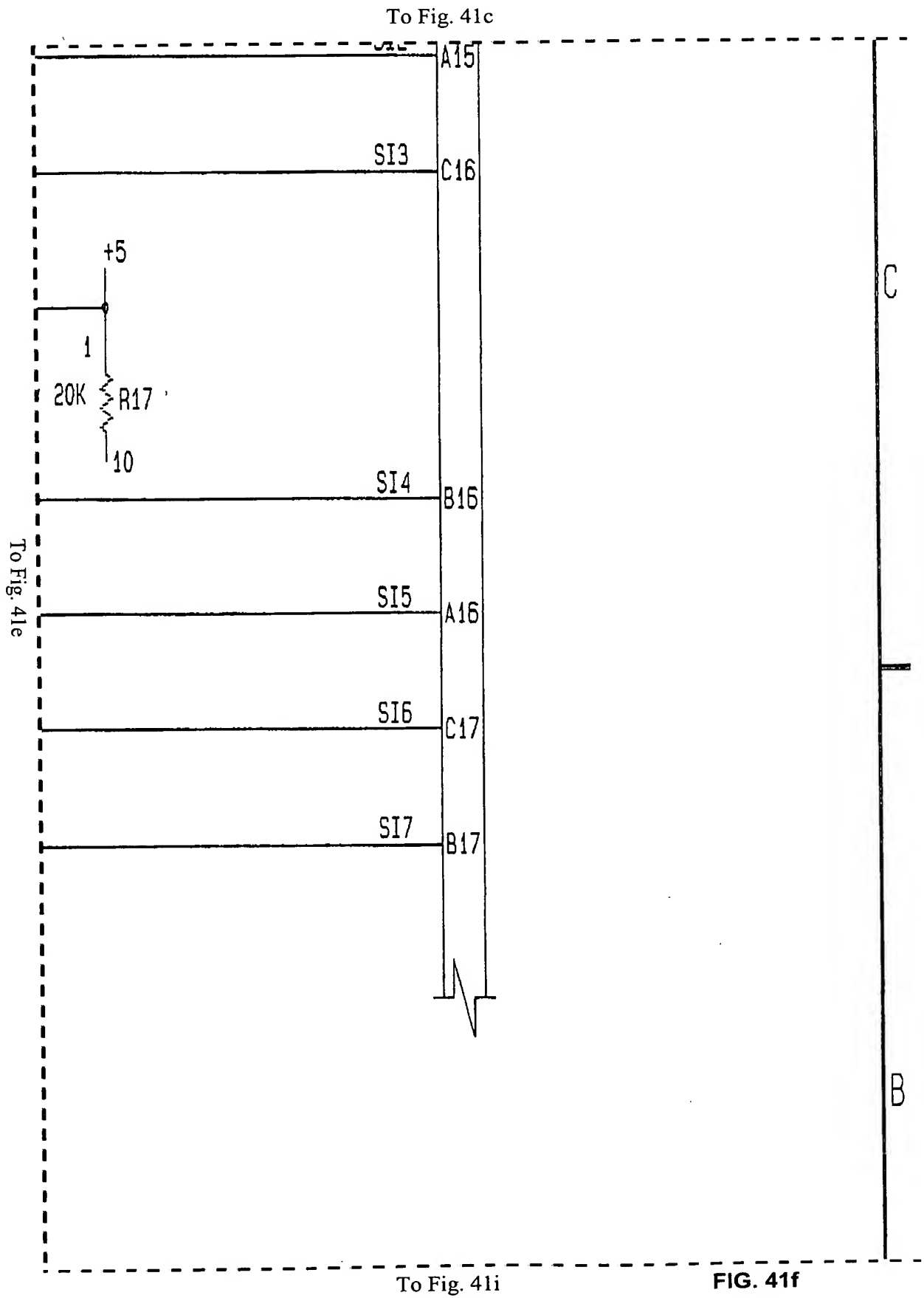
FIG. 41d

To Fig. 41b



To Fig. 41h

FIG. 41e



To Fig. 41d

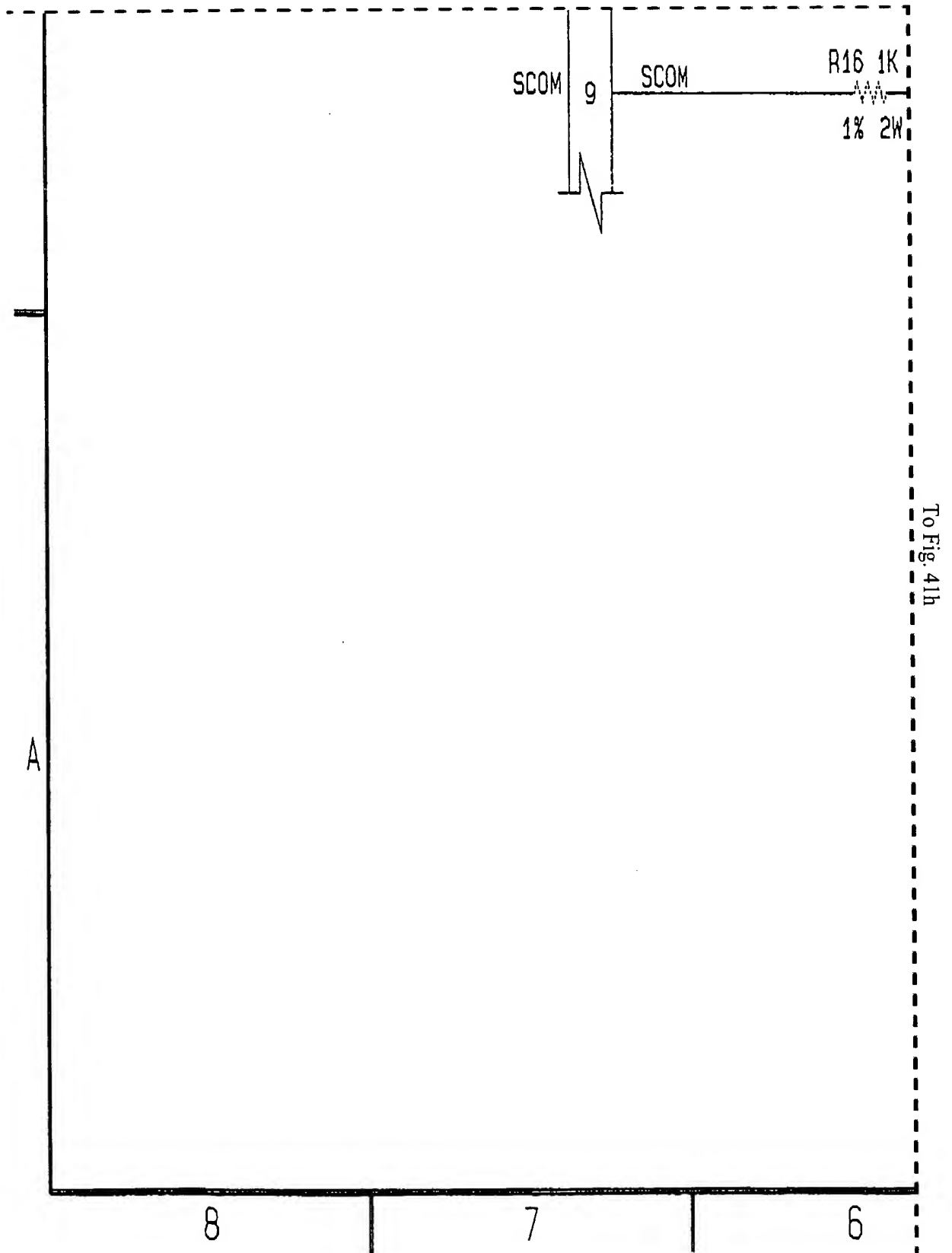


FIG. 41g

To Fig. 41e

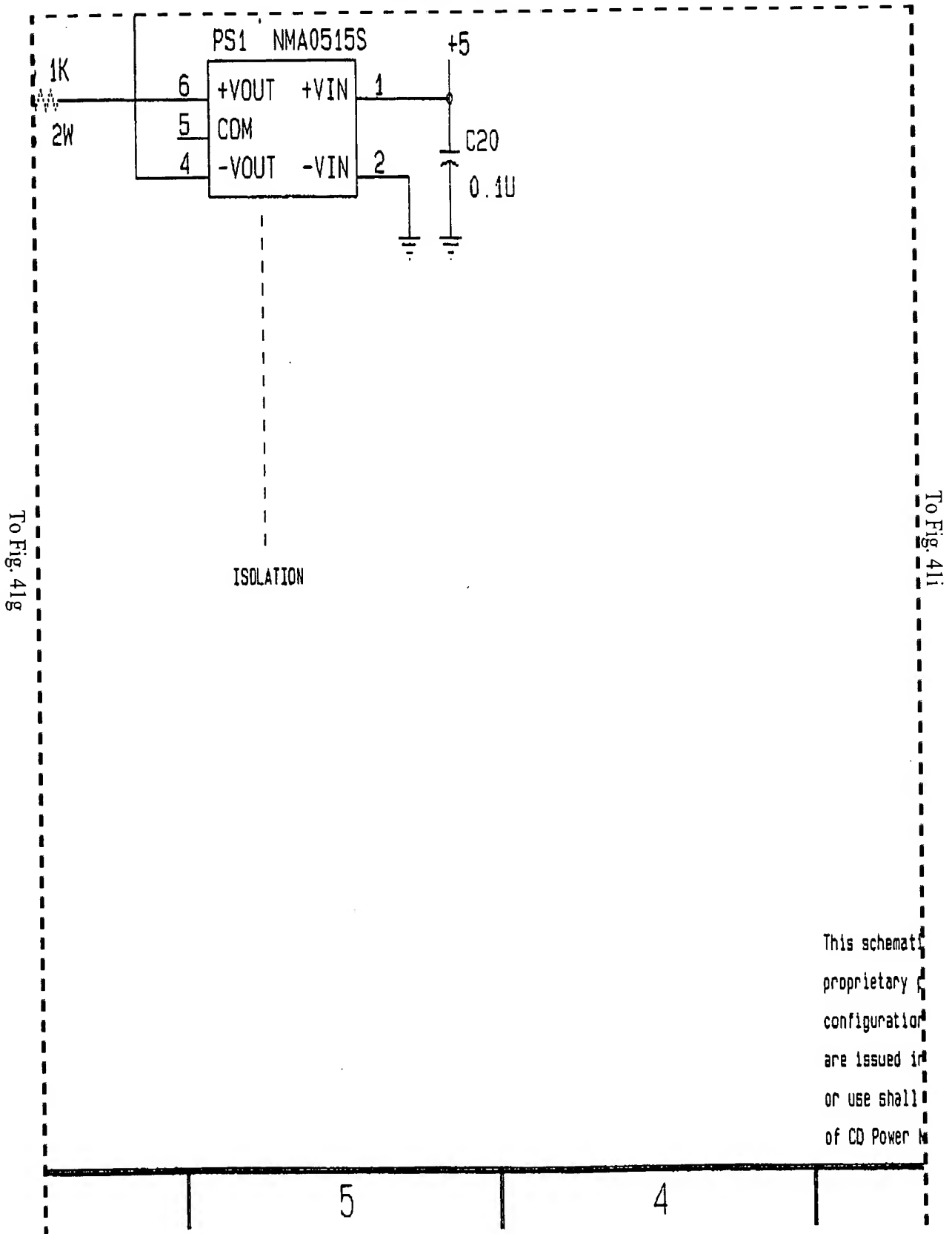


FIG. 41h

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To Fig. 41f

To Fig. 41h

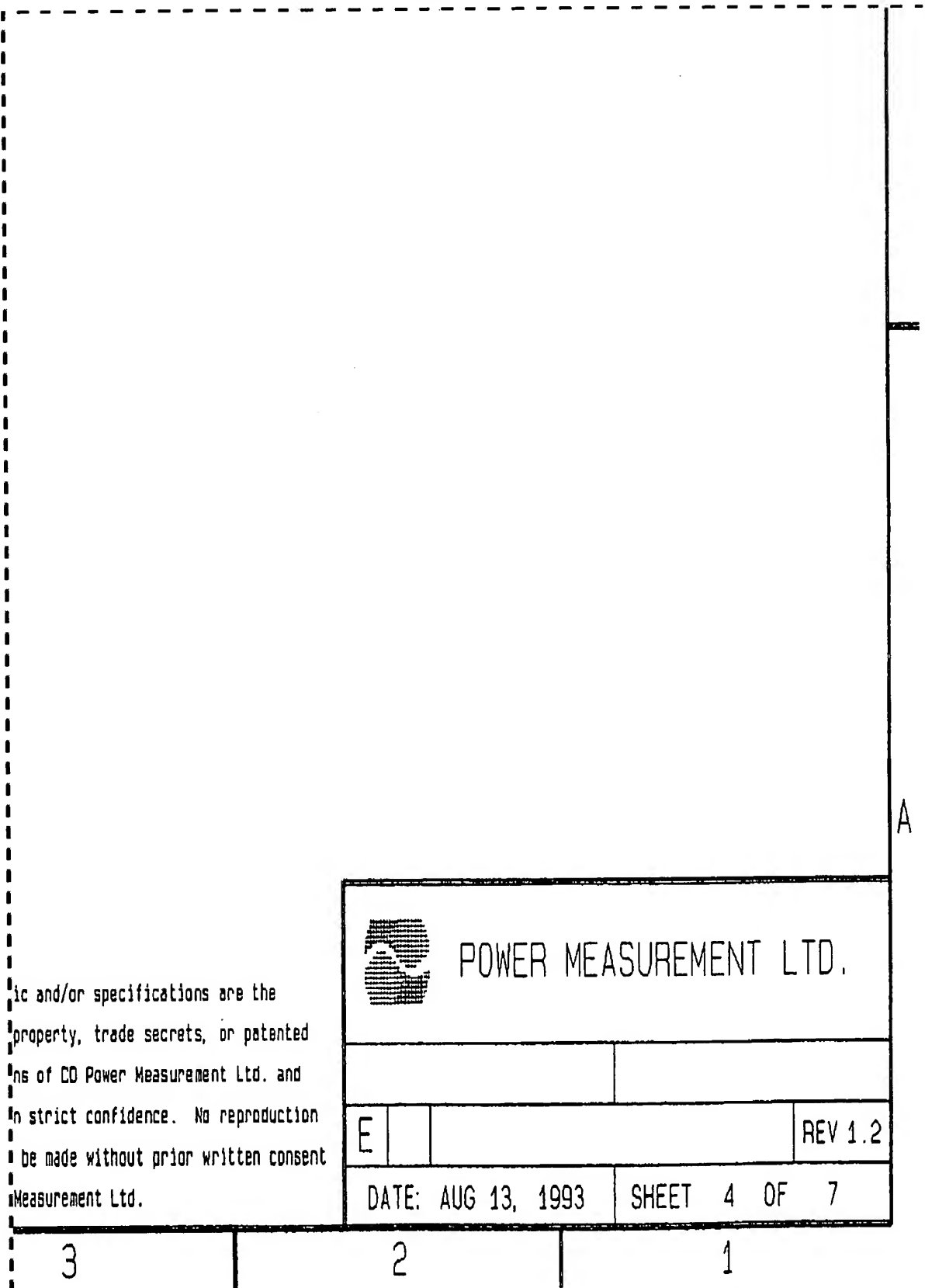
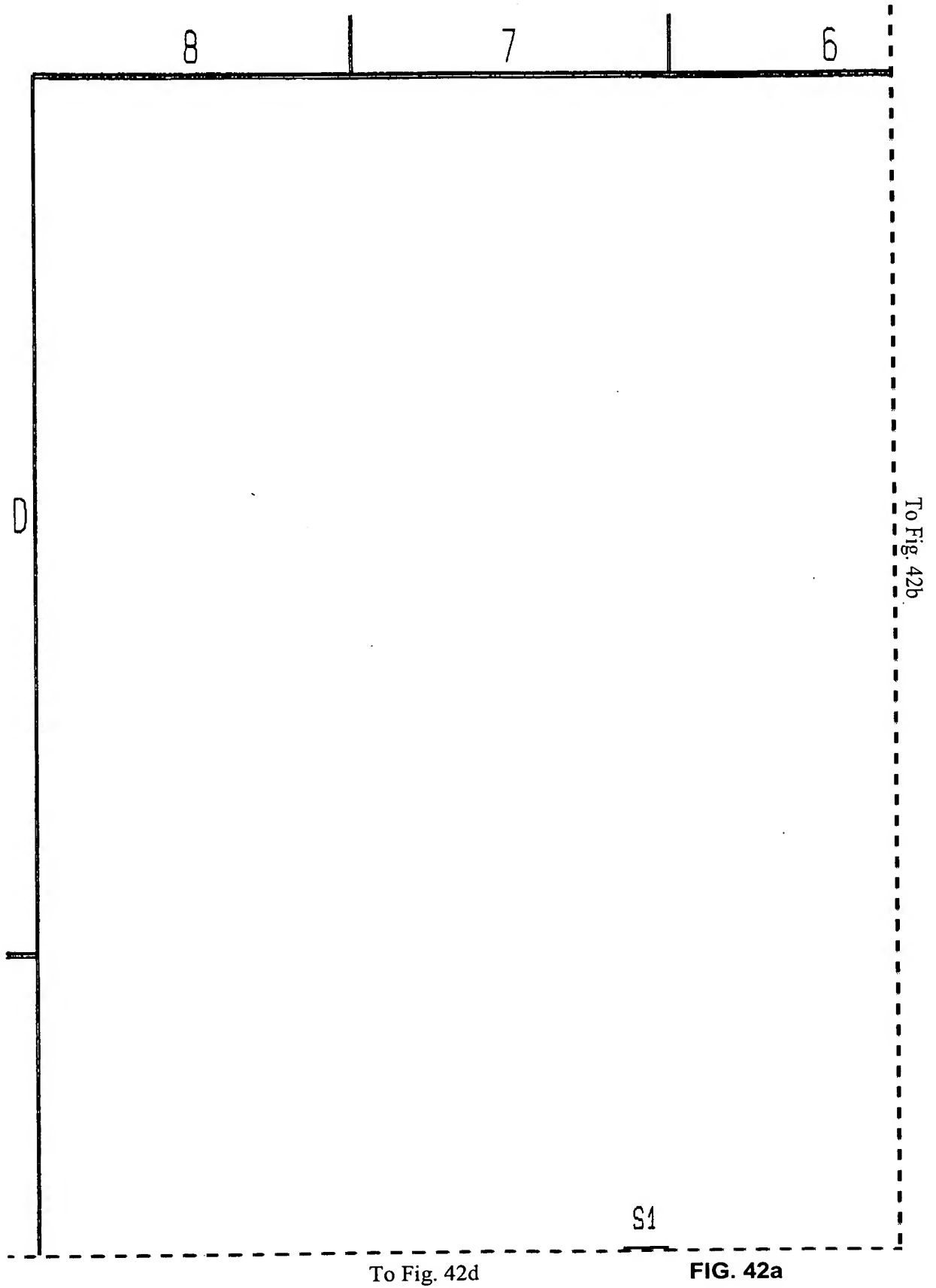
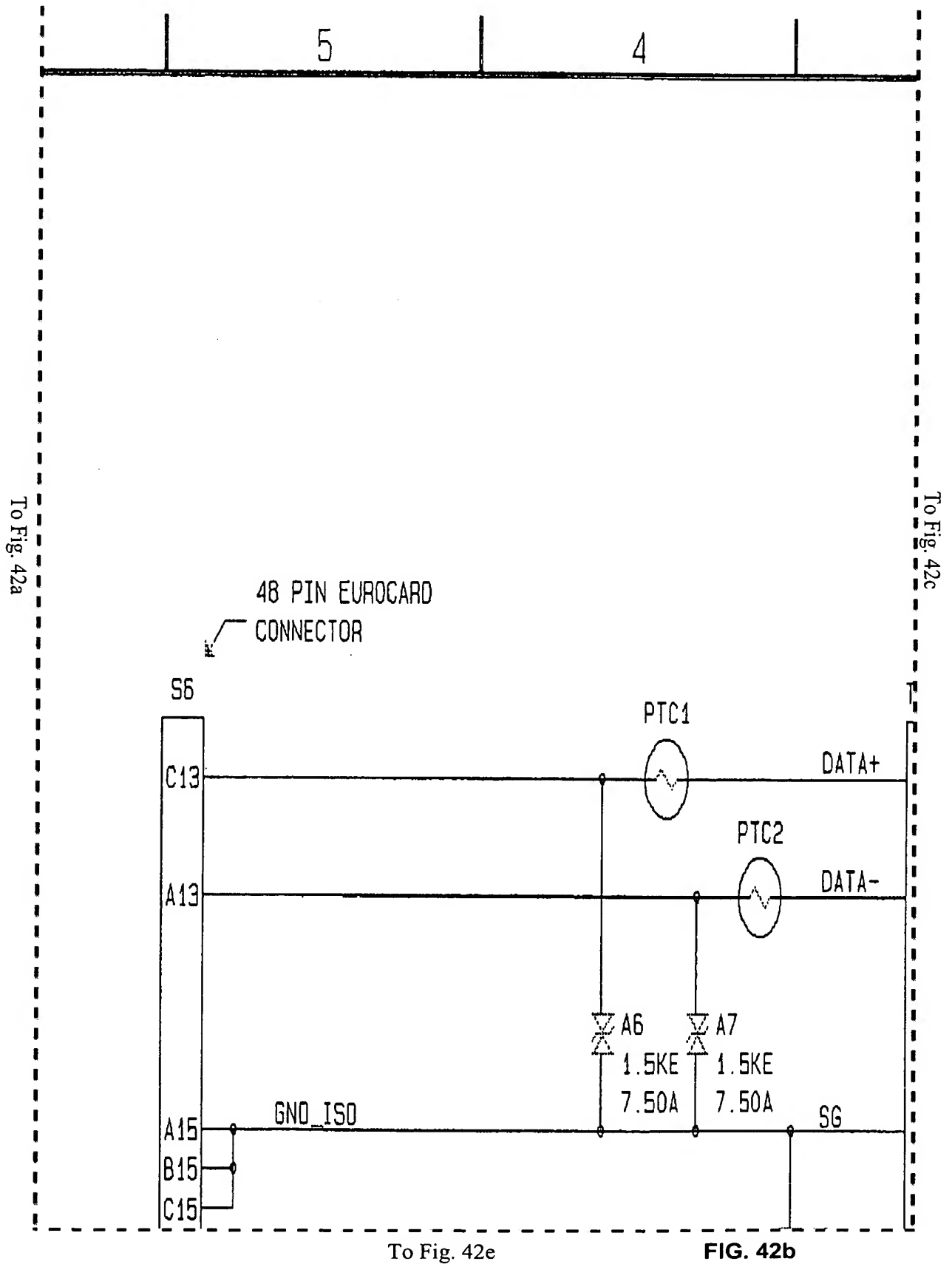
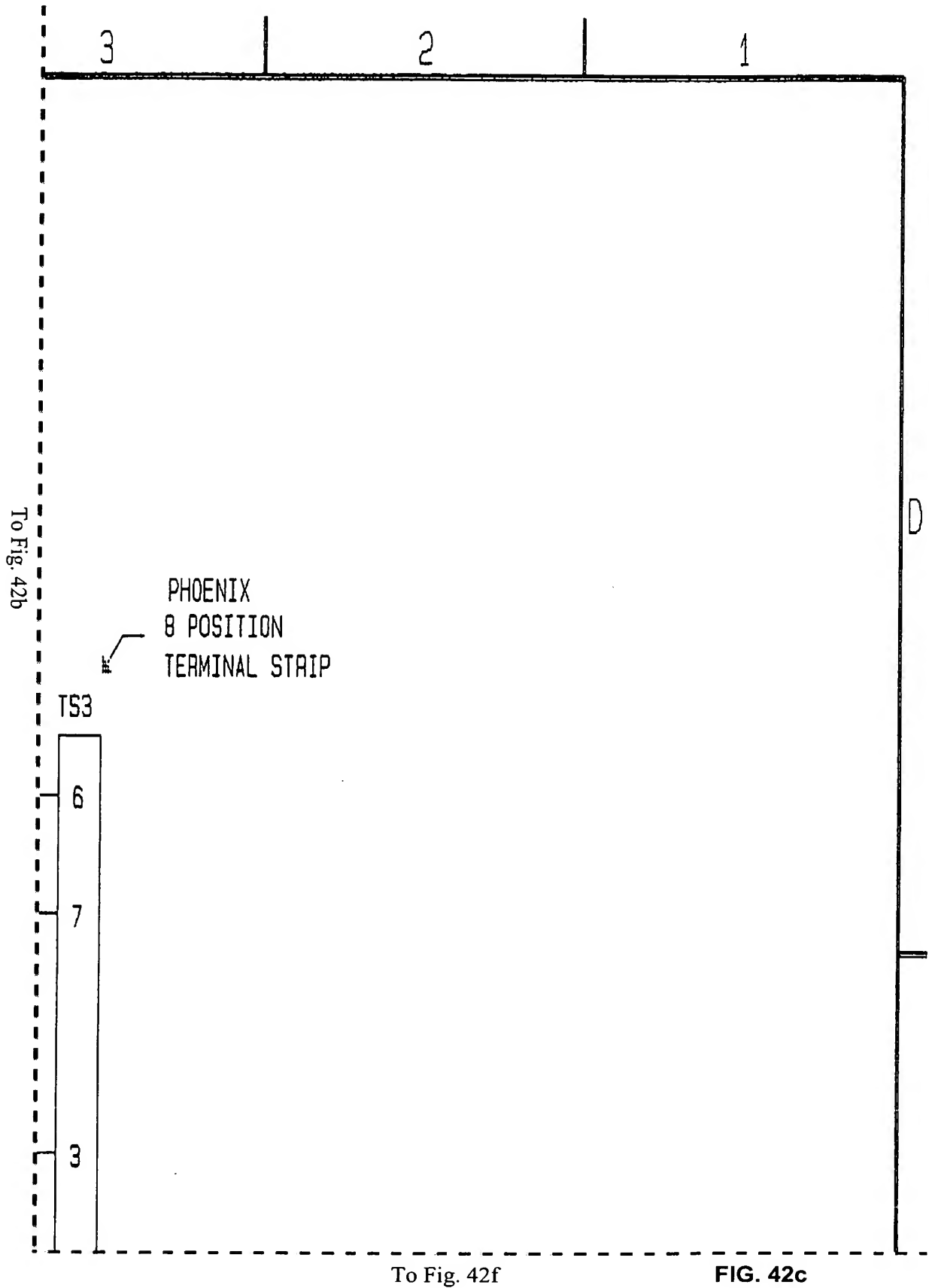


FIG. 41i







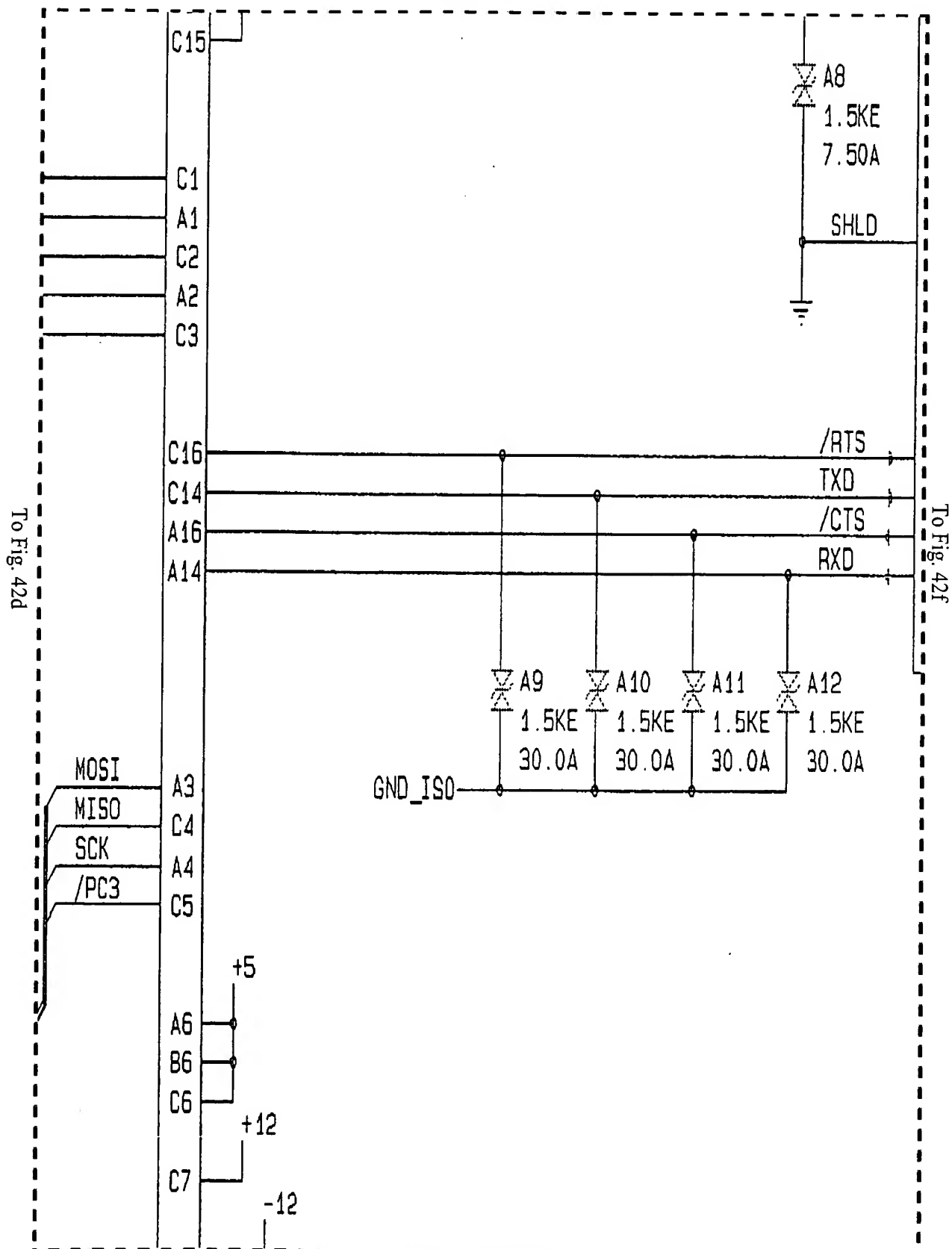
TO/FROM SHT 2

QSPI BUS

To Fig. 42c

FIG. 42d

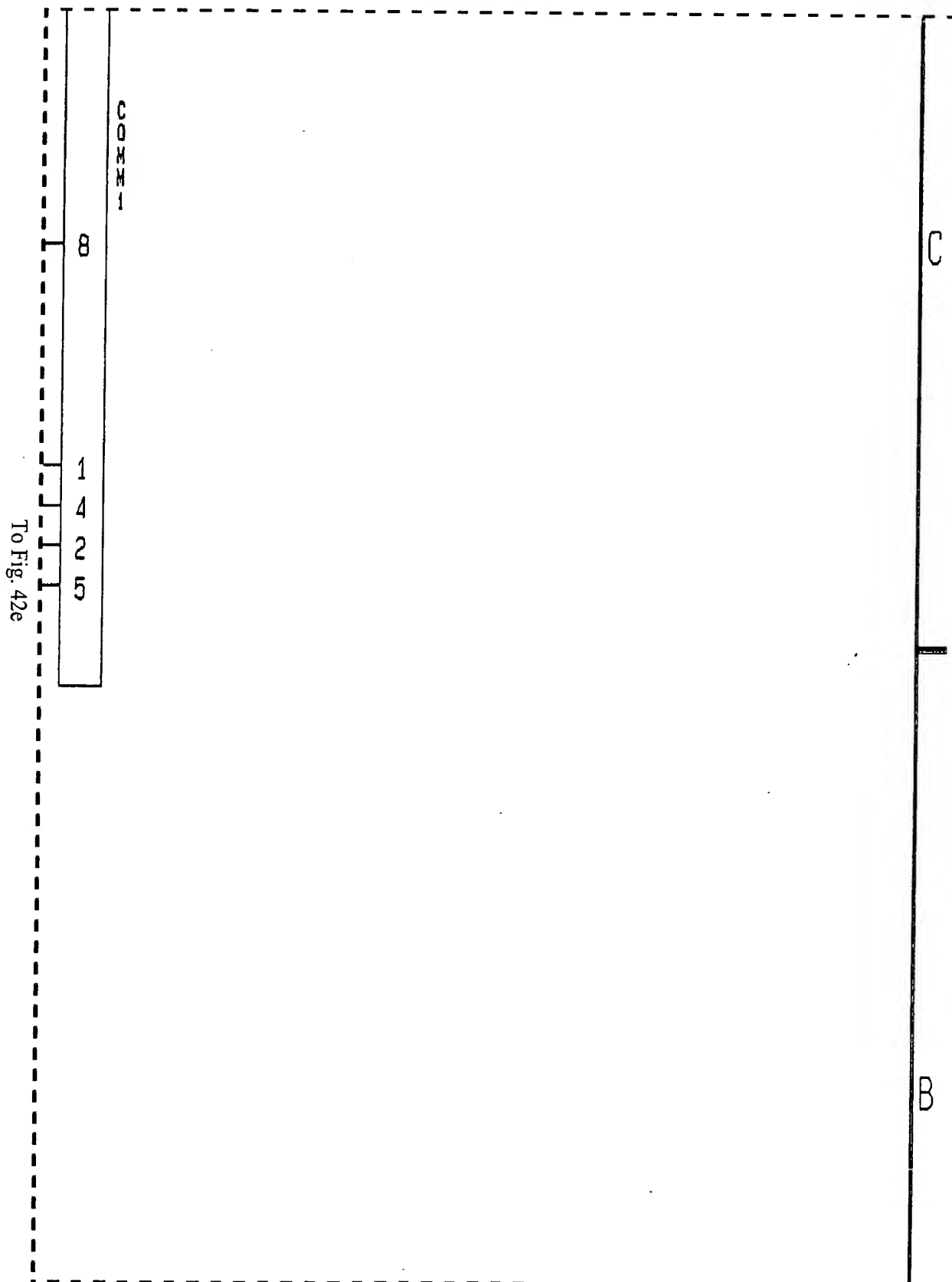
To Fig. 42b



To Fig. 42h

FIG. 42e

To Fig. 42c



To Fig. 42i

FIG. 42f

To Fig. 42d

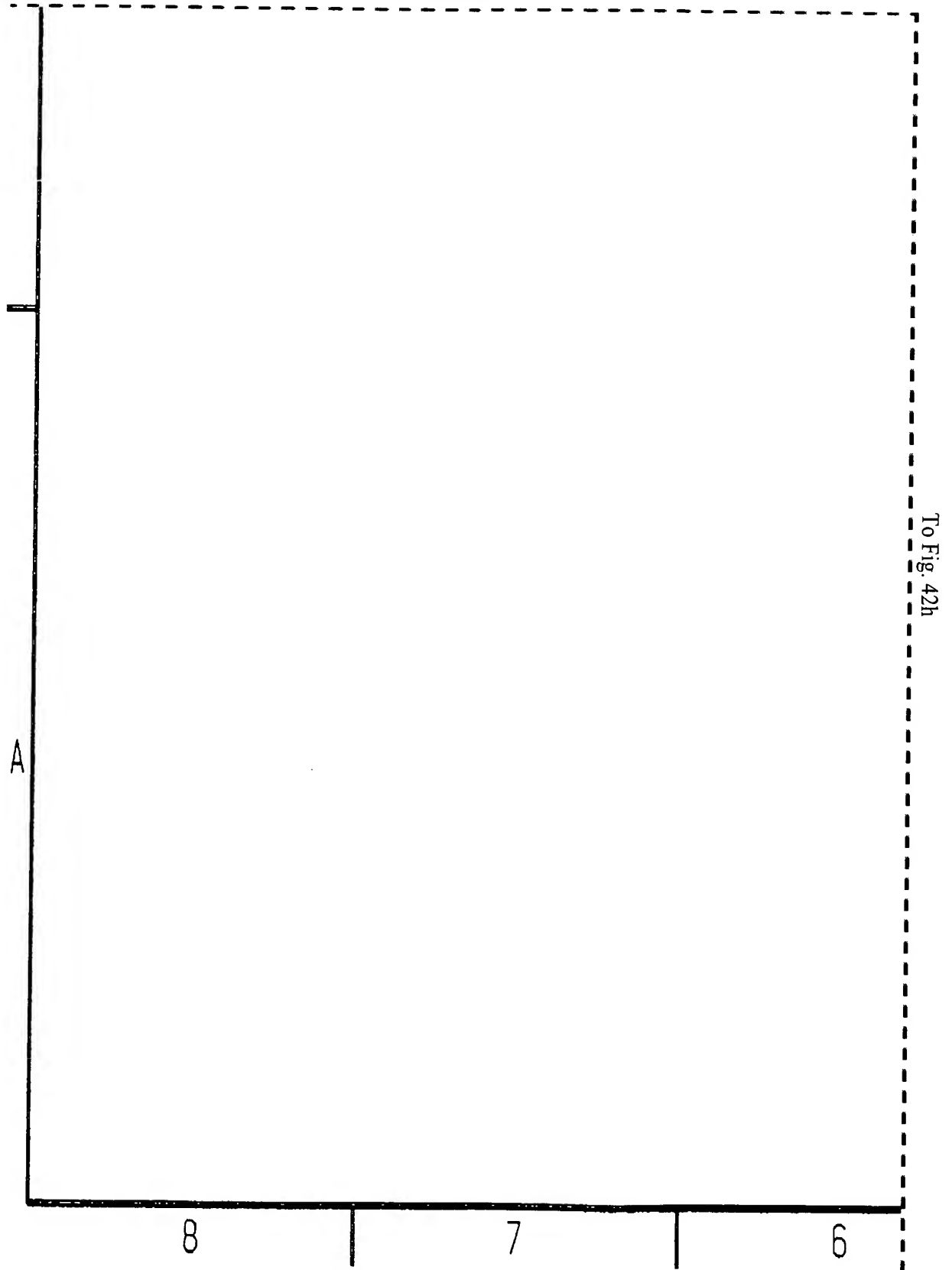


FIG. 42g

To Fig. 42e

To Fig. 42g

To Fig. 42i

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FIG. 42h

To Fig. 42f

To Fig. 42h

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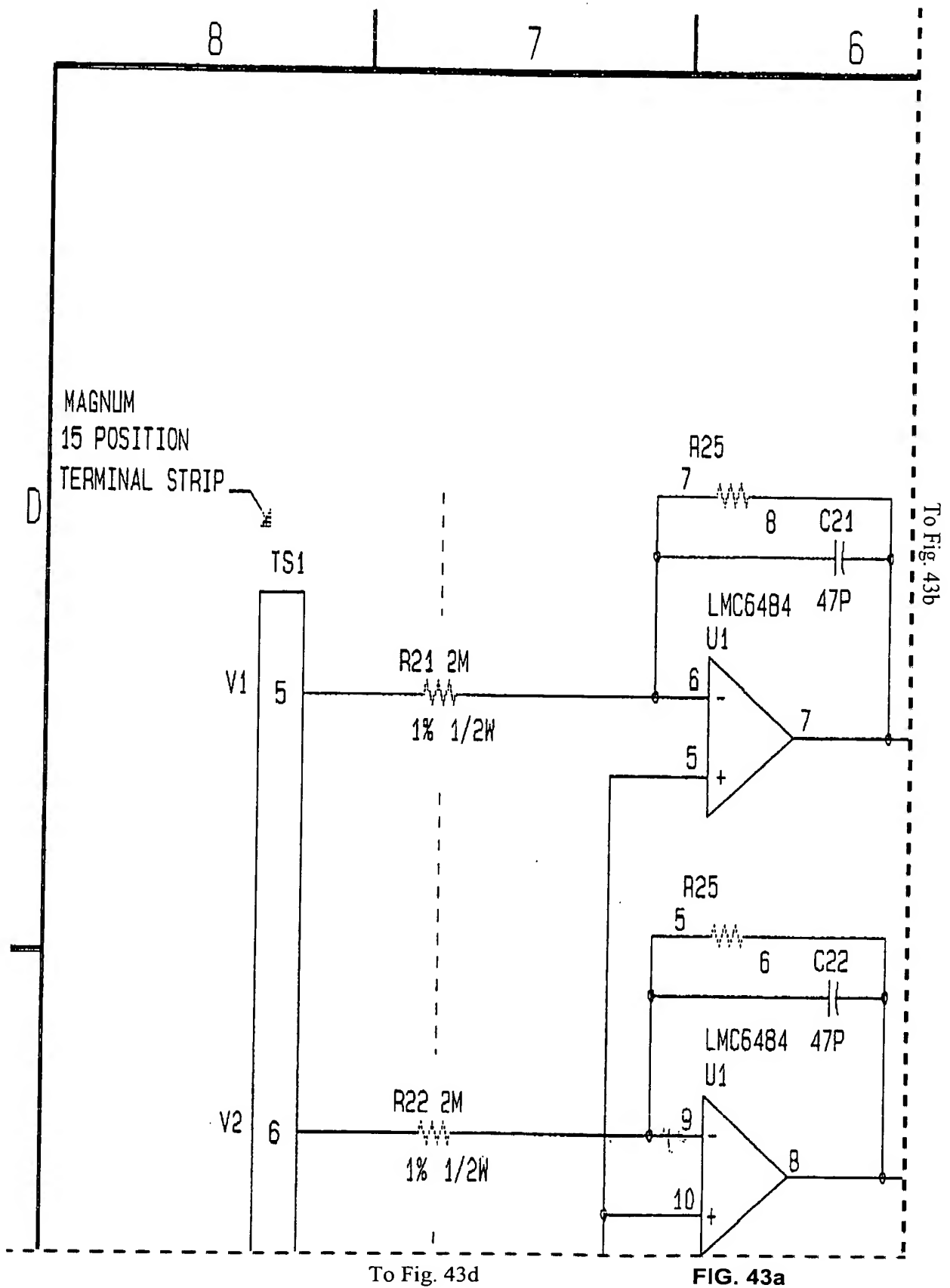
SHEET 5 OF 7

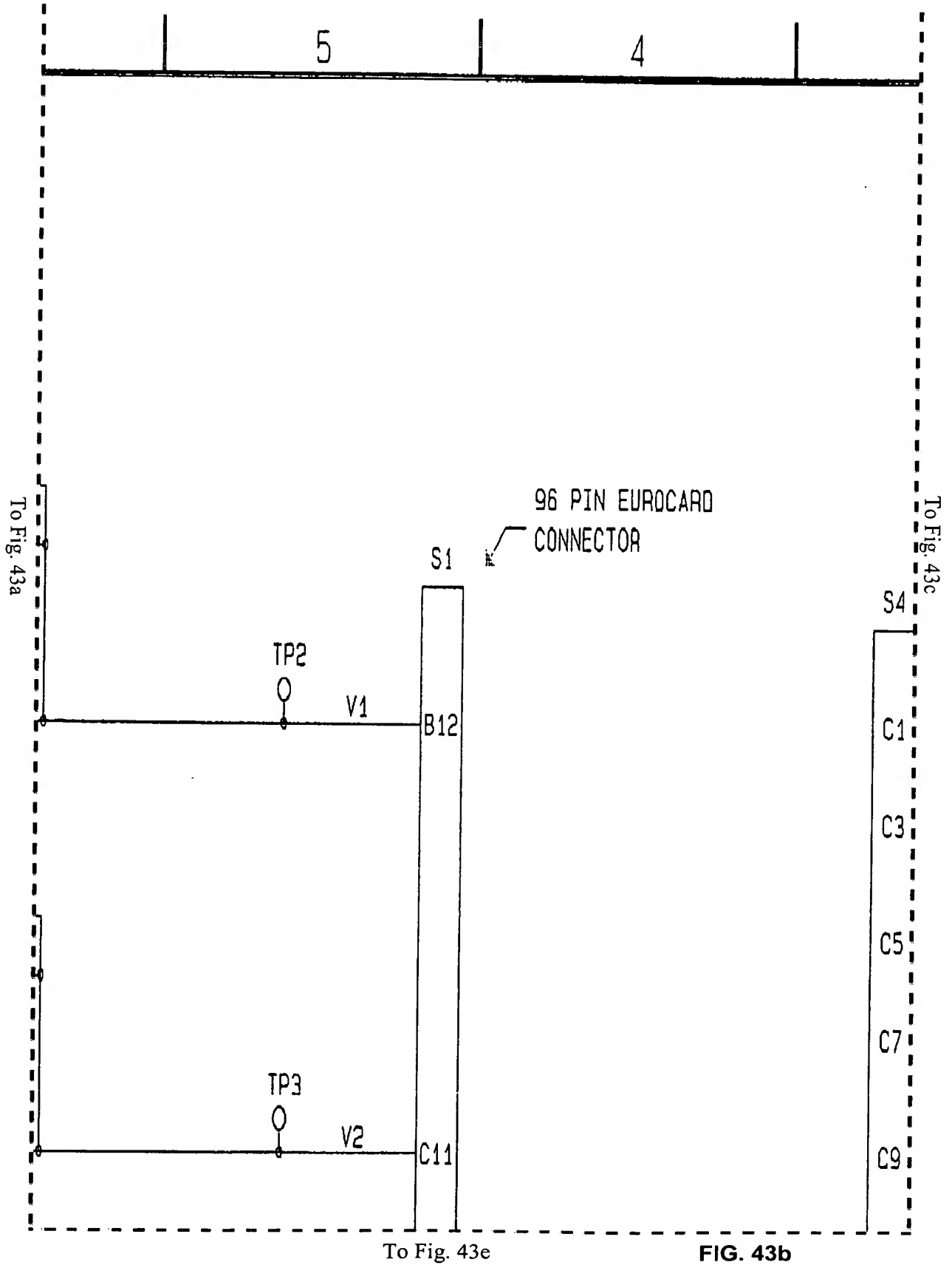
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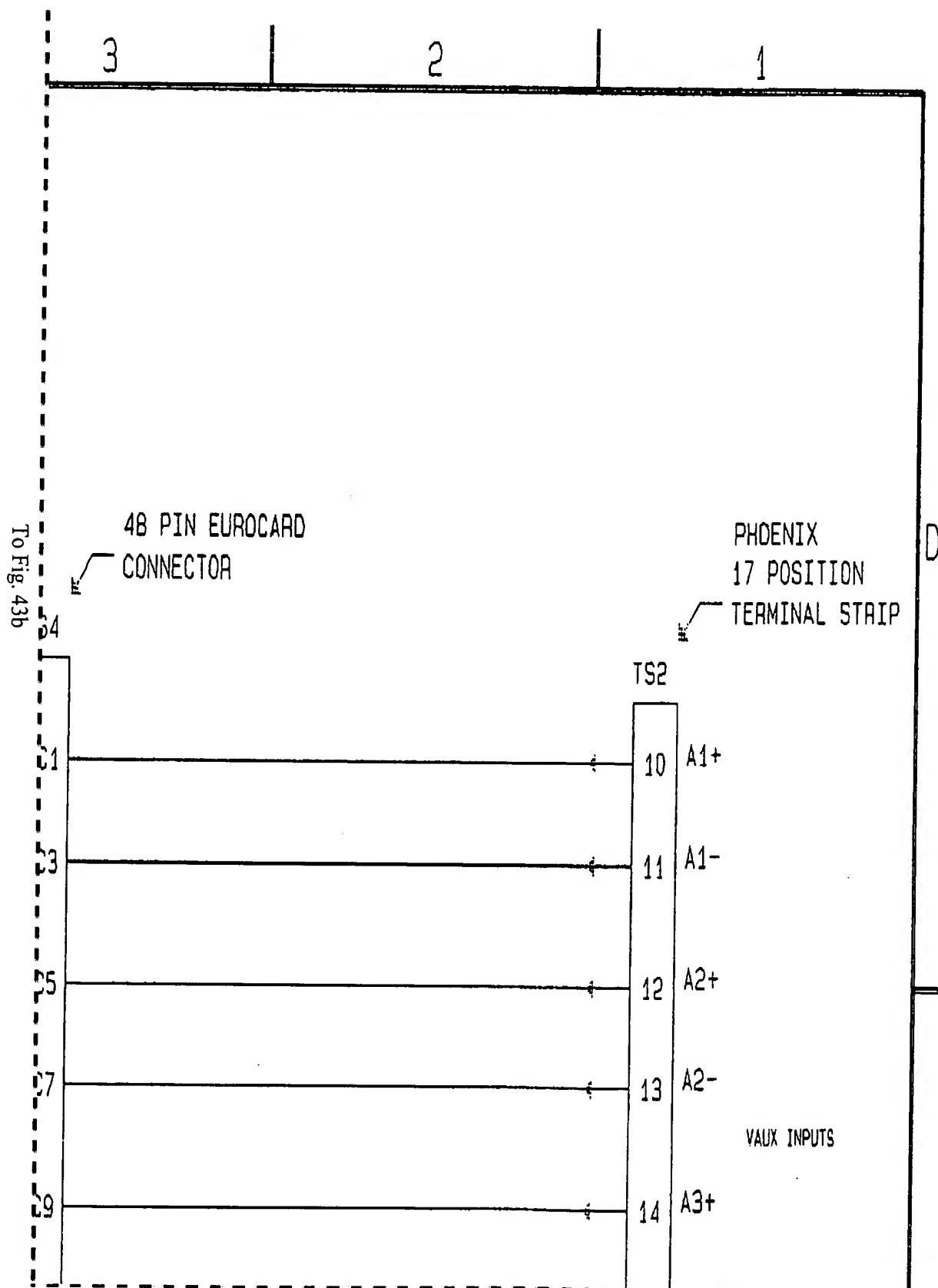
2

1

FIG. 42i

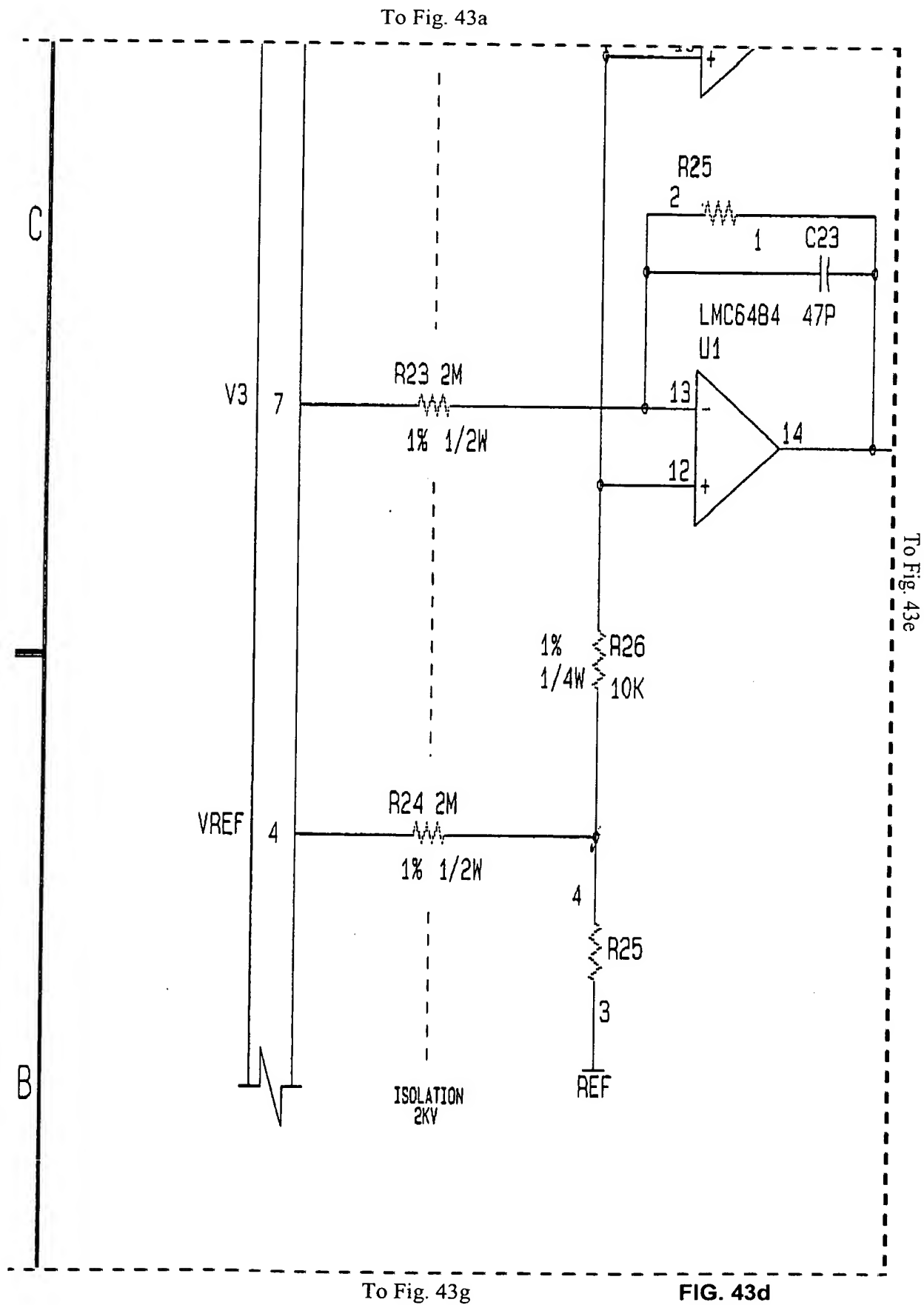




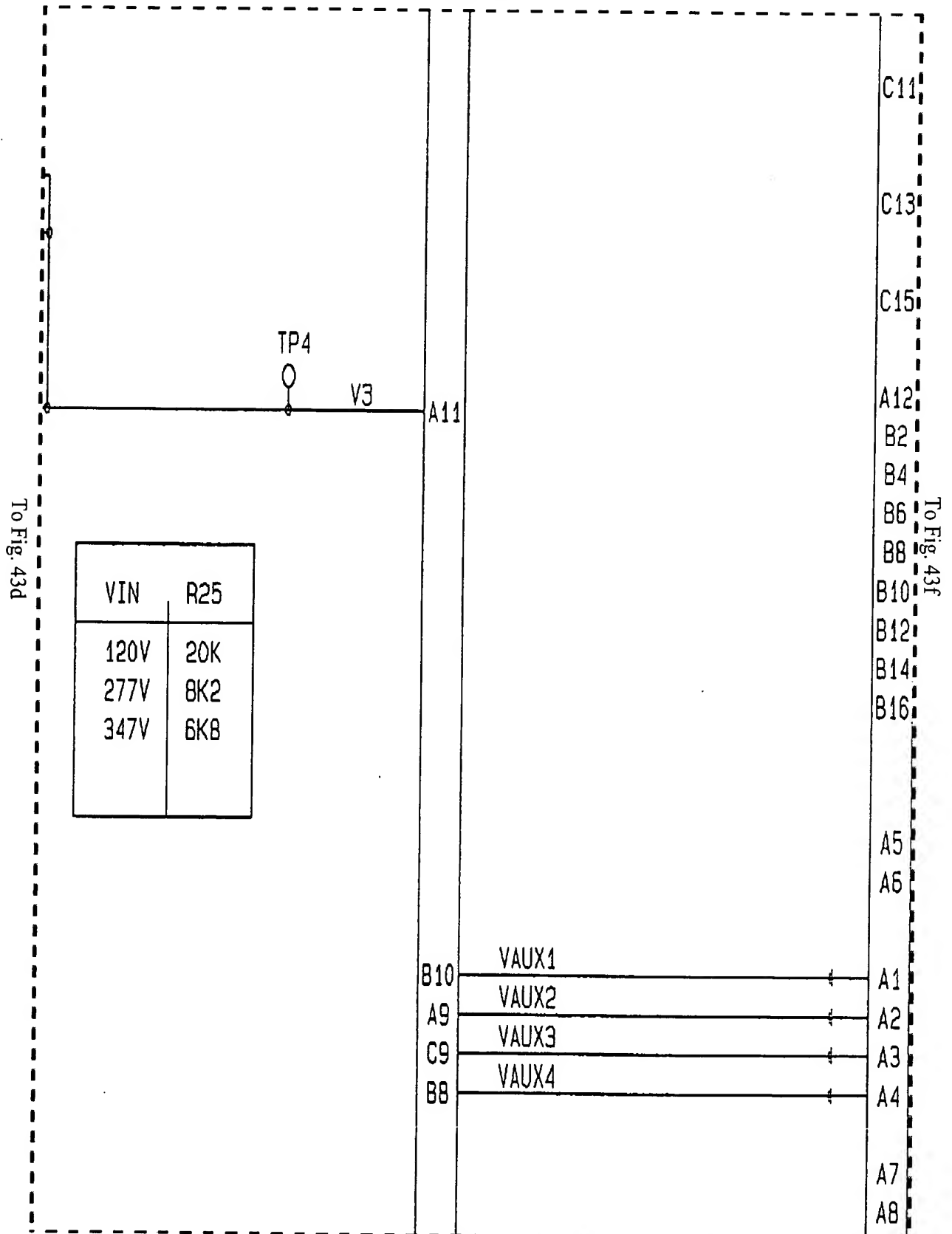


To Fig. 43f

FIG. 43c



To Fig. 43b



To Fig. 43h

FIG. 43e

The schematic diagram illustrates a multi-channel signal processing circuit. It features a vertical bus labeled 'B' on the right side. A horizontal dashed line at the top indicates a connection to another component. The circuit includes several input channels, each represented by a horizontal line connecting to the bus. These channels are labeled as follows:

- Channel 1: Labeled 'A3-' with terminal numbers 11 and 15.
- Channel 2: Labeled 'A4+' with terminal numbers 13 and 16.
- Channel 3: Labeled 'A4-' with terminal numbers 15 and 17.

A ground symbol is connected to the bottom of the bus. On the left side, there is a series of terminals numbered 1 through 18. These terminals are connected to various components:

- Terminals 12 through 16 are connected to a common ground line.
- Terminal 15 is connected to a component labeled '+5'.
- Terminal 16 is connected to a component labeled '+12'.
- Terminal 17 is connected to a component labeled '+12'.
- Terminal 18 is connected to a component labeled '+12'.

The diagram also shows a reference to 'To Fig. 43e' near the bottom left corner.

FIG. 43f

To Fig. 43d

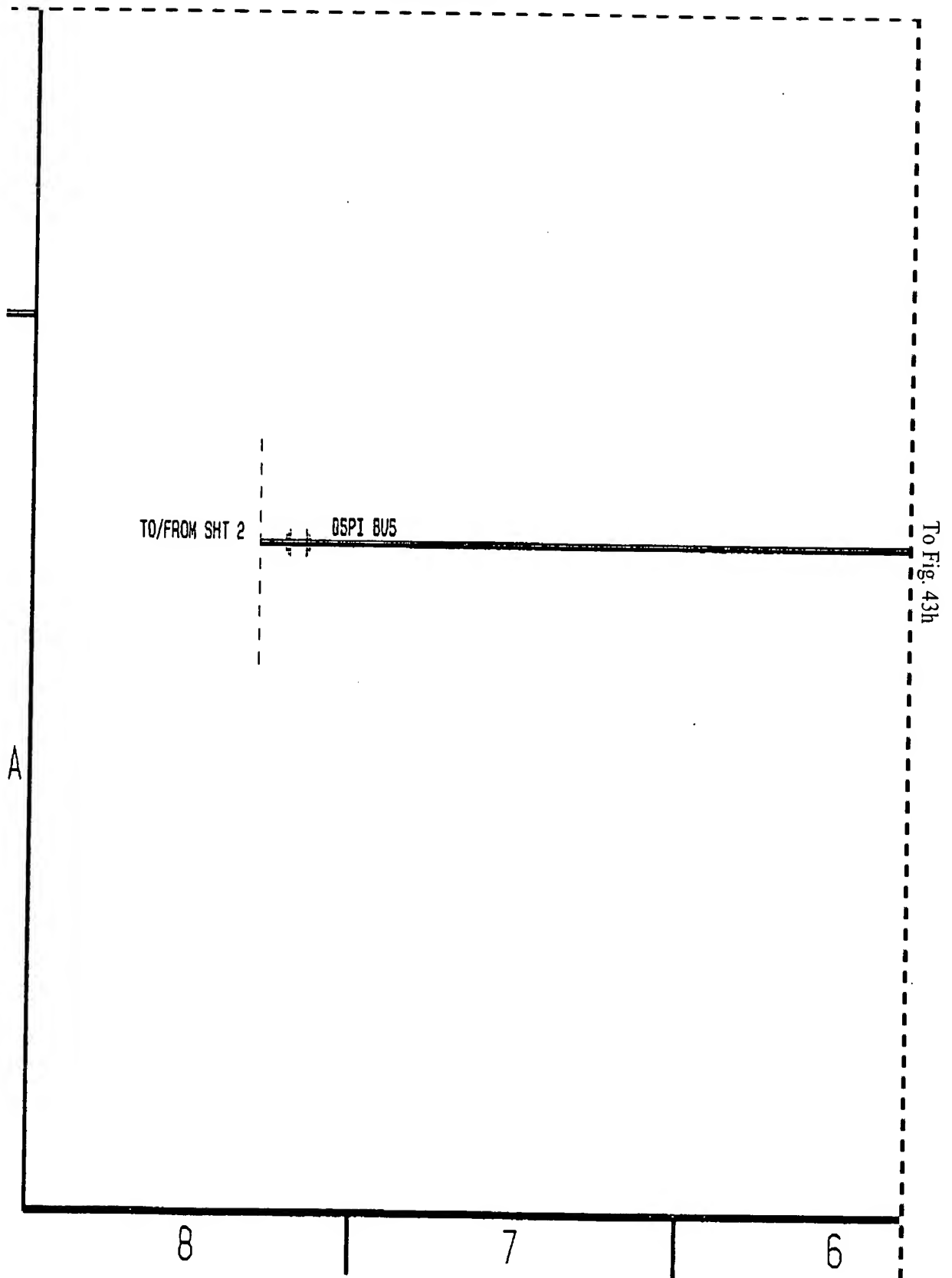


FIG. 43g

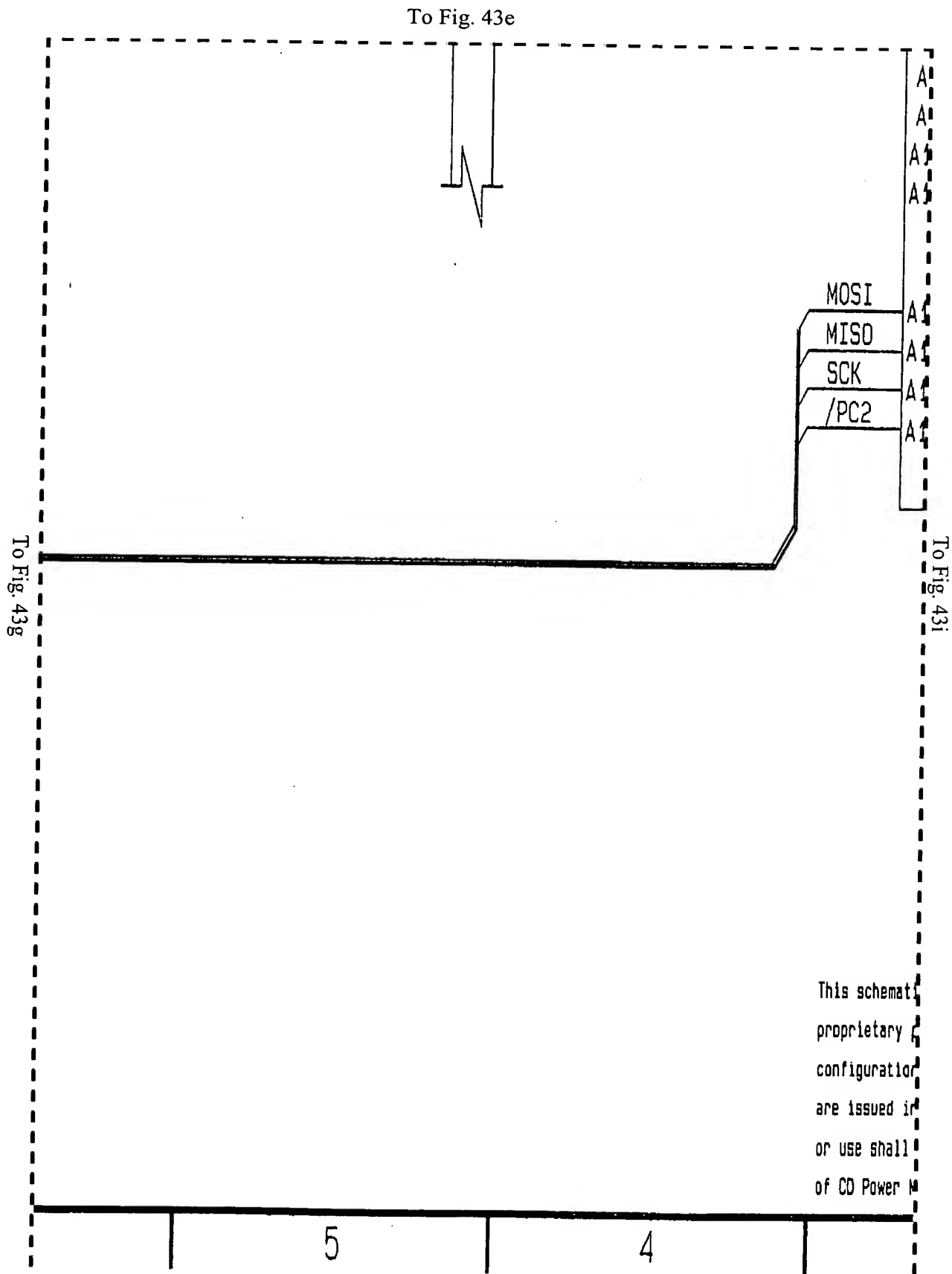


FIG. 43h

To Fig. 43f

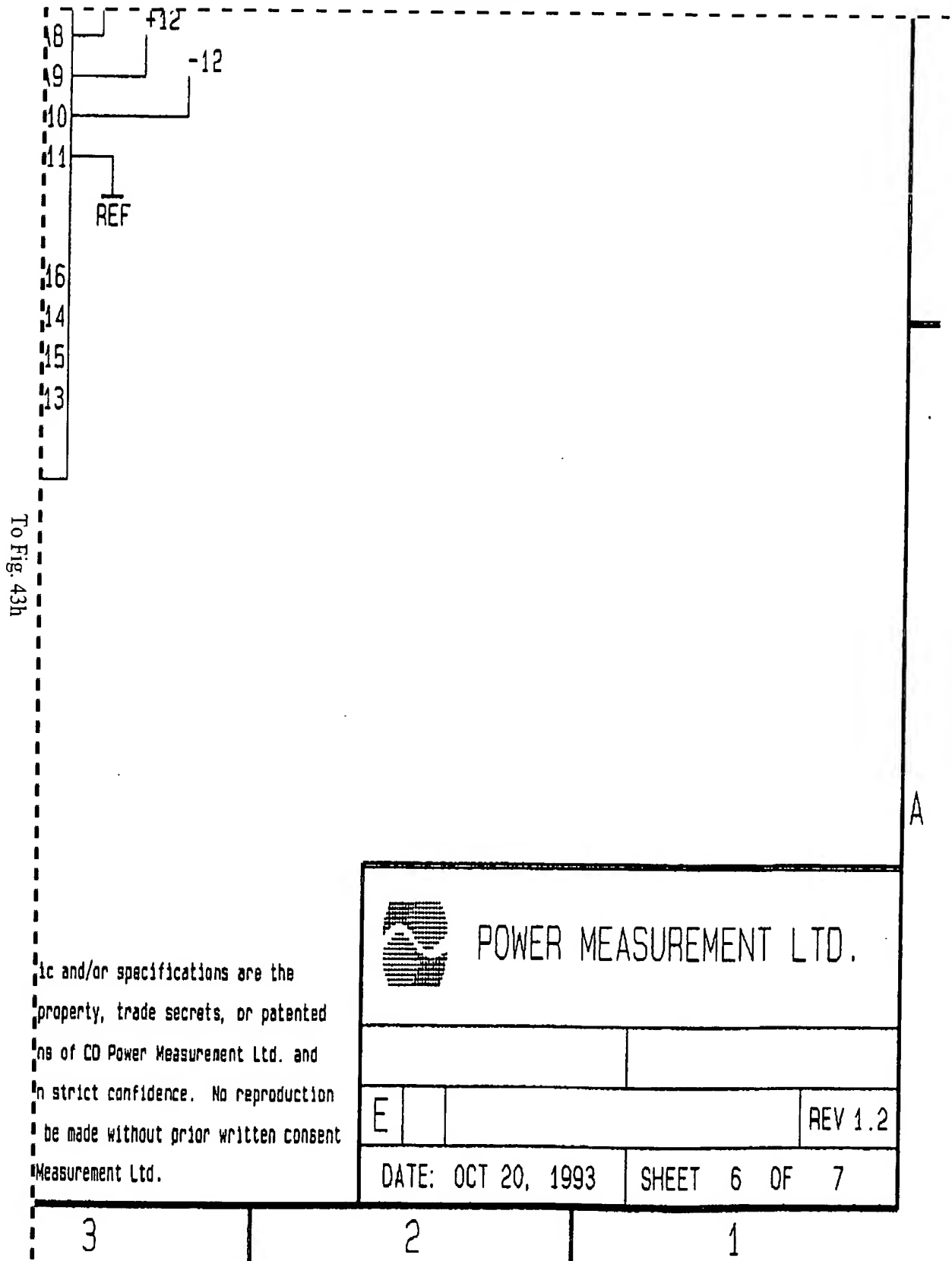
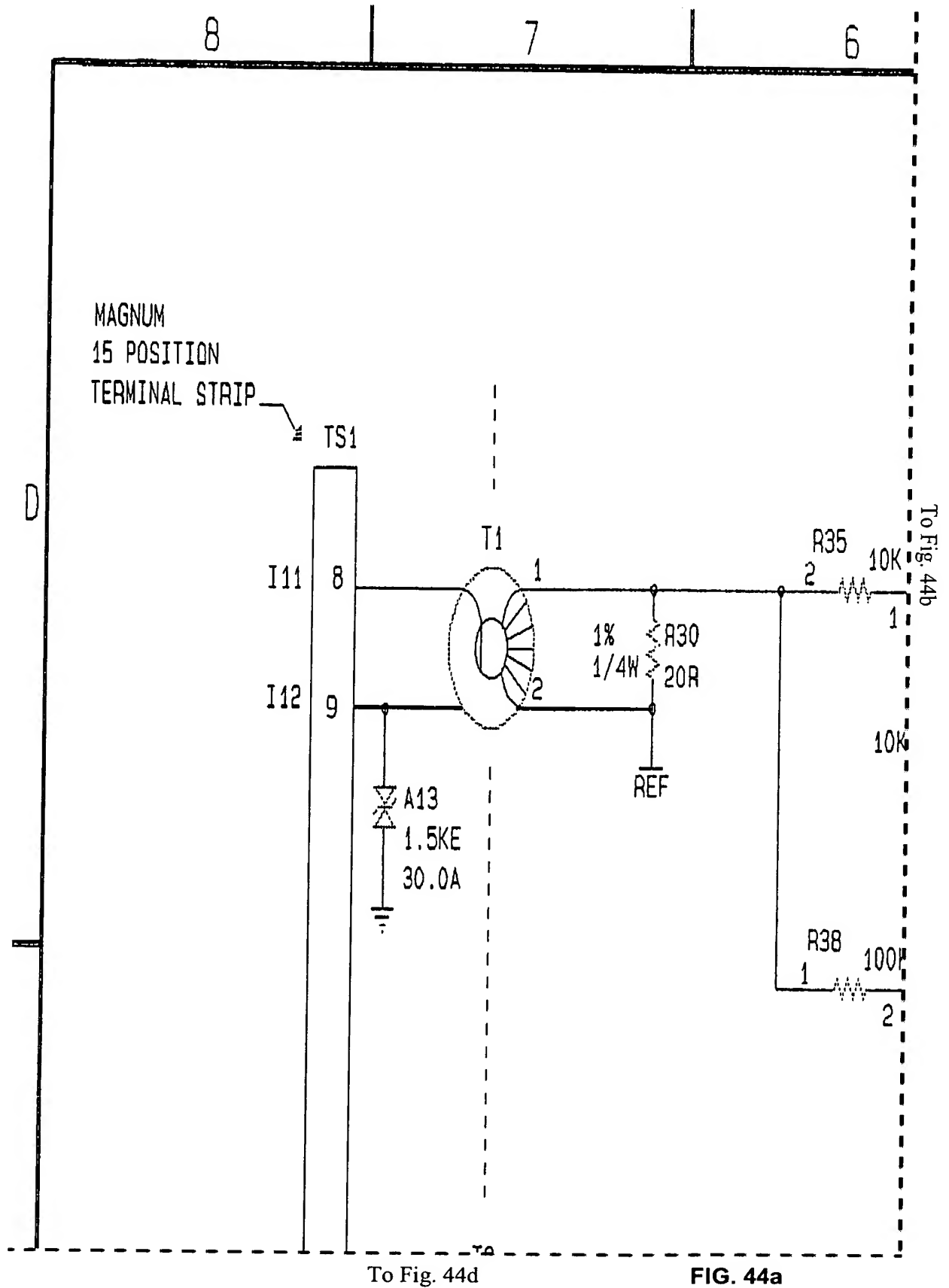
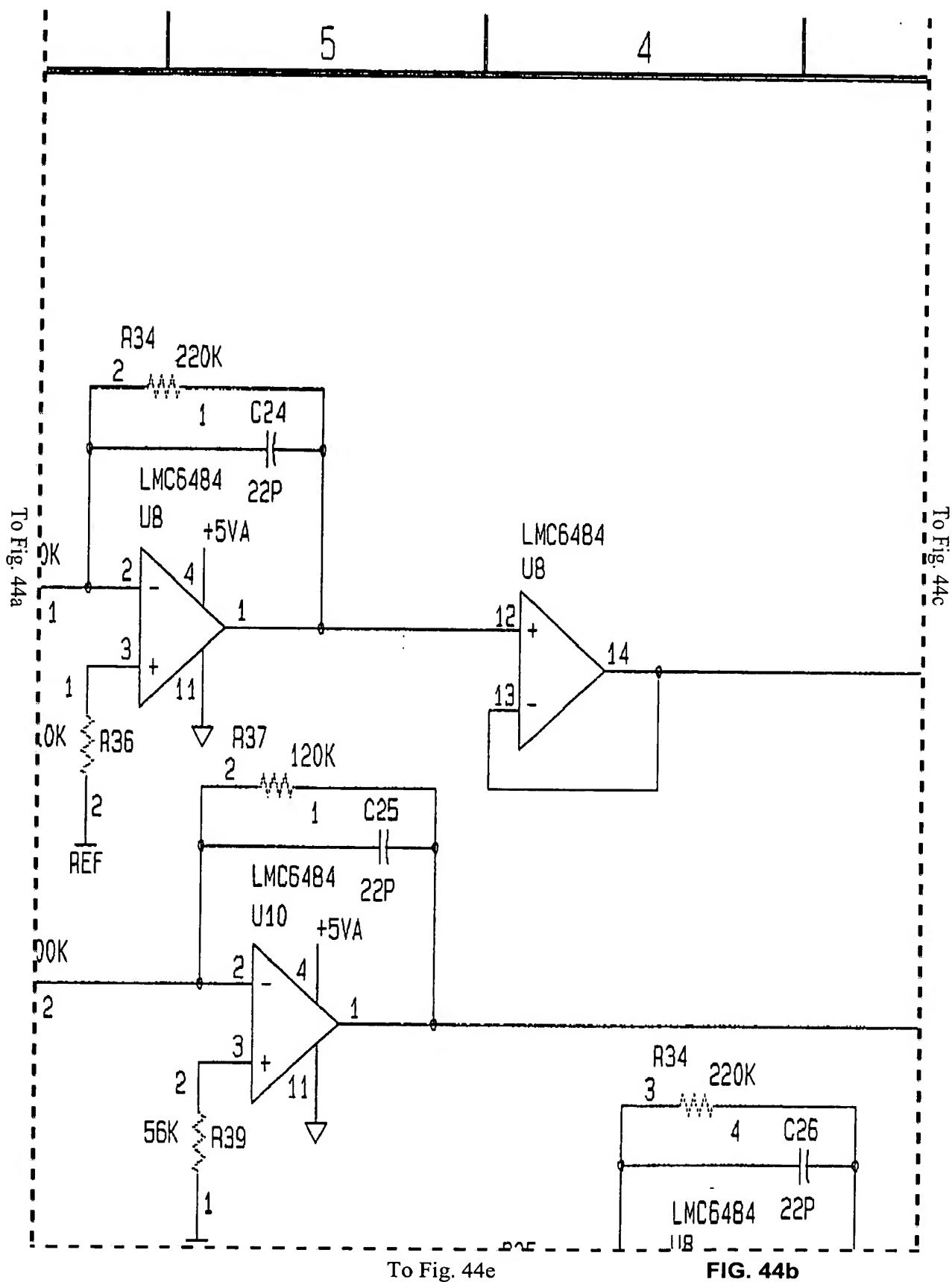


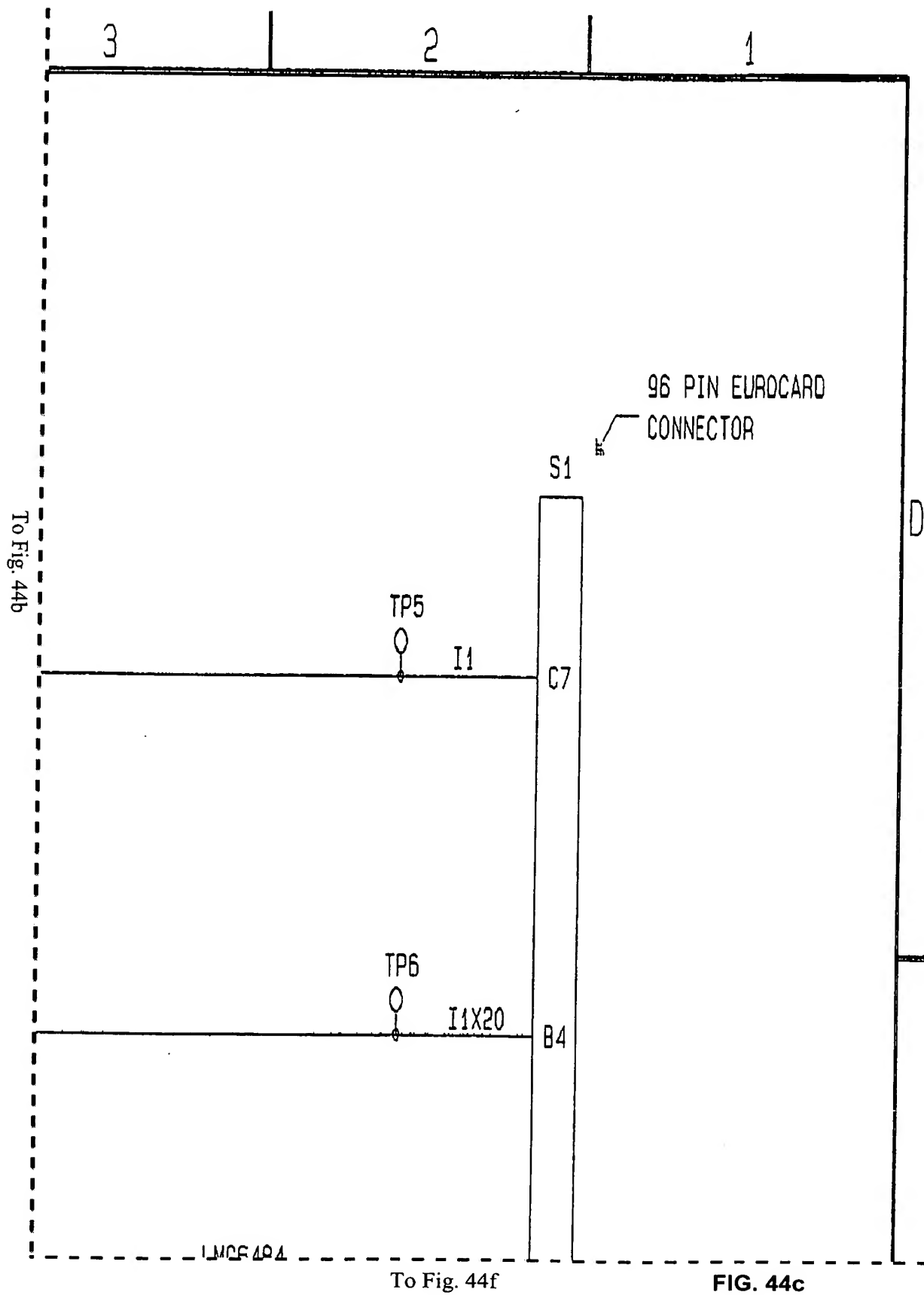
FIG. 43i

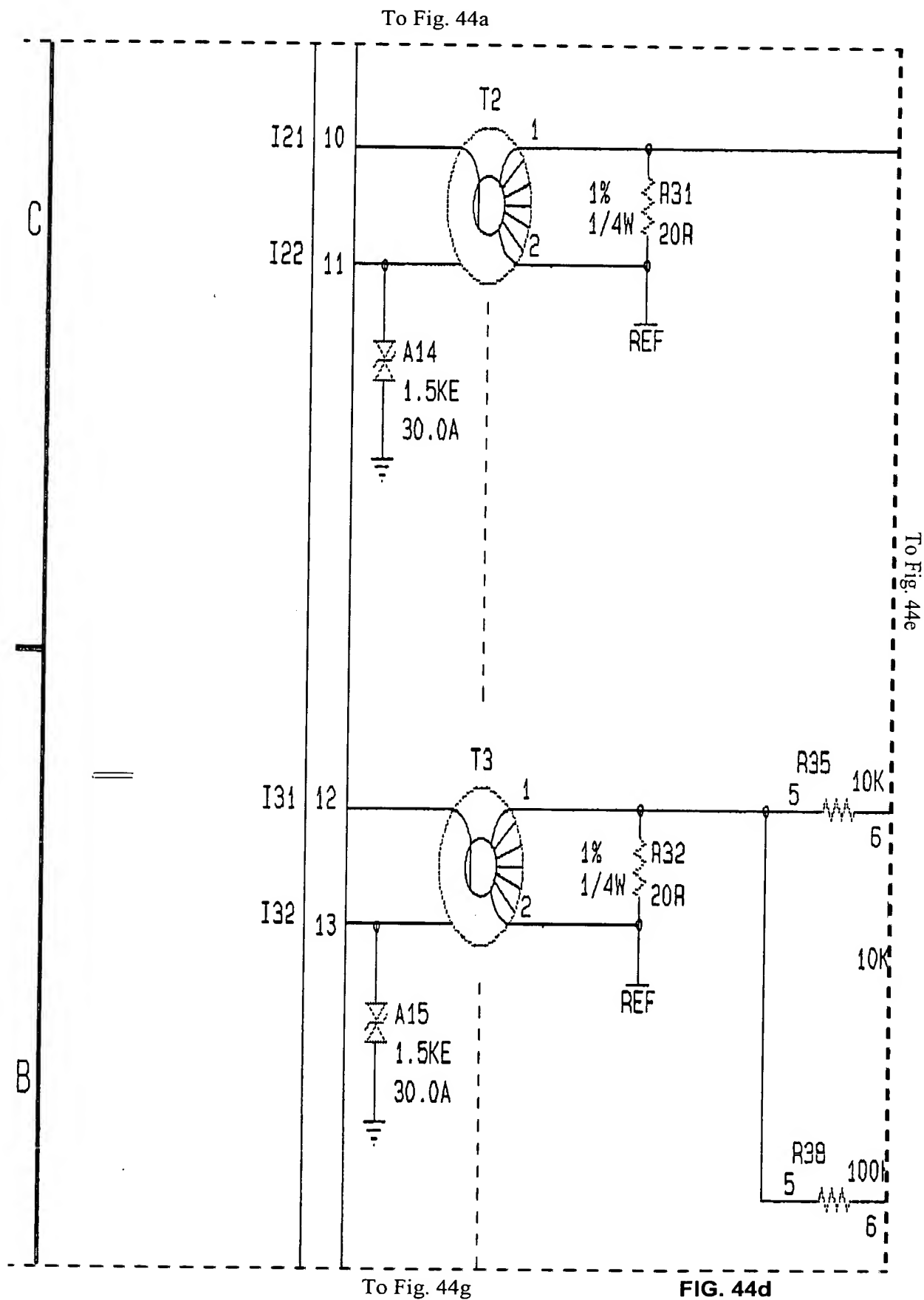




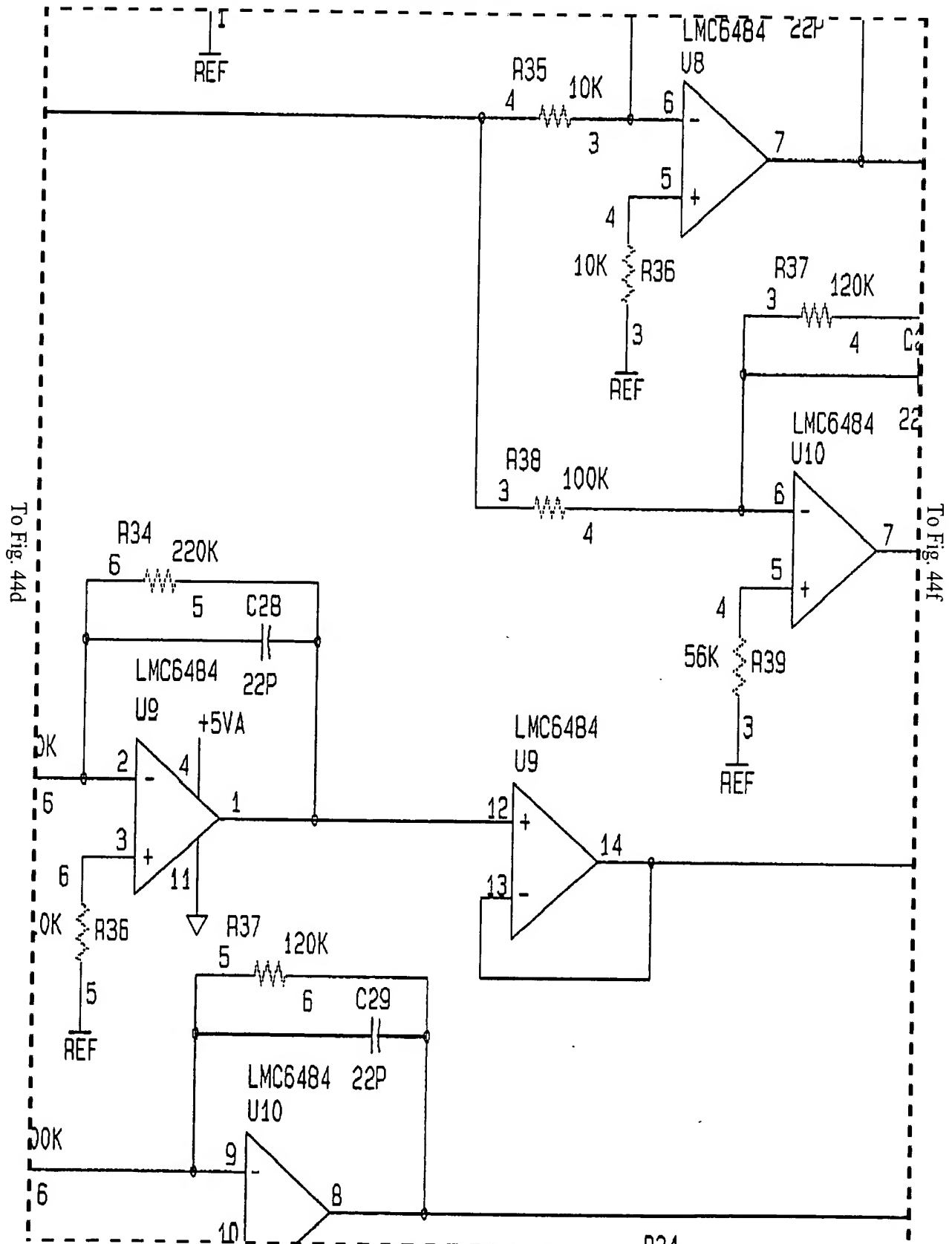
To Fig. 44e

FIG. 44b



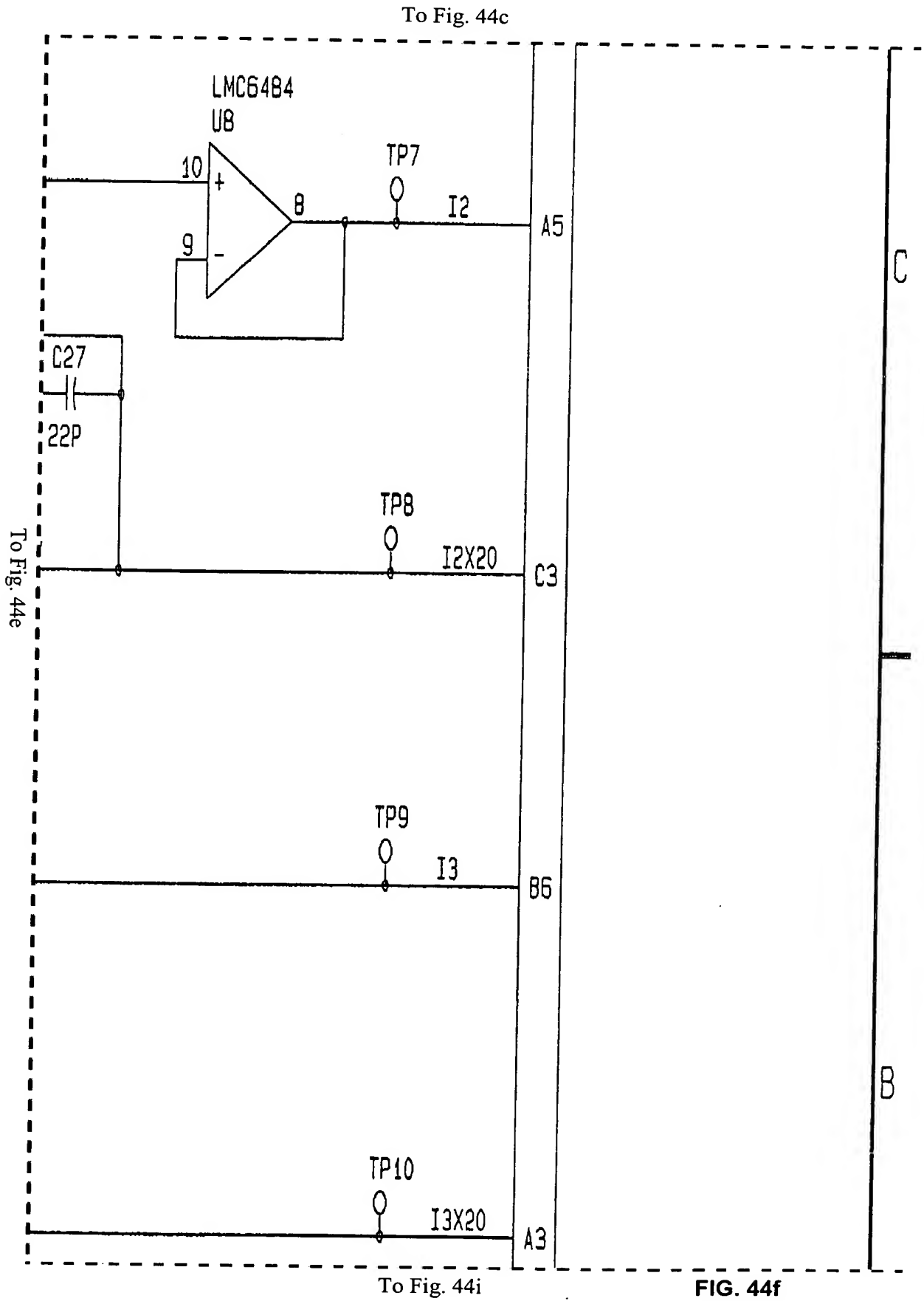


To Fig. 44b



To Fig. 44h

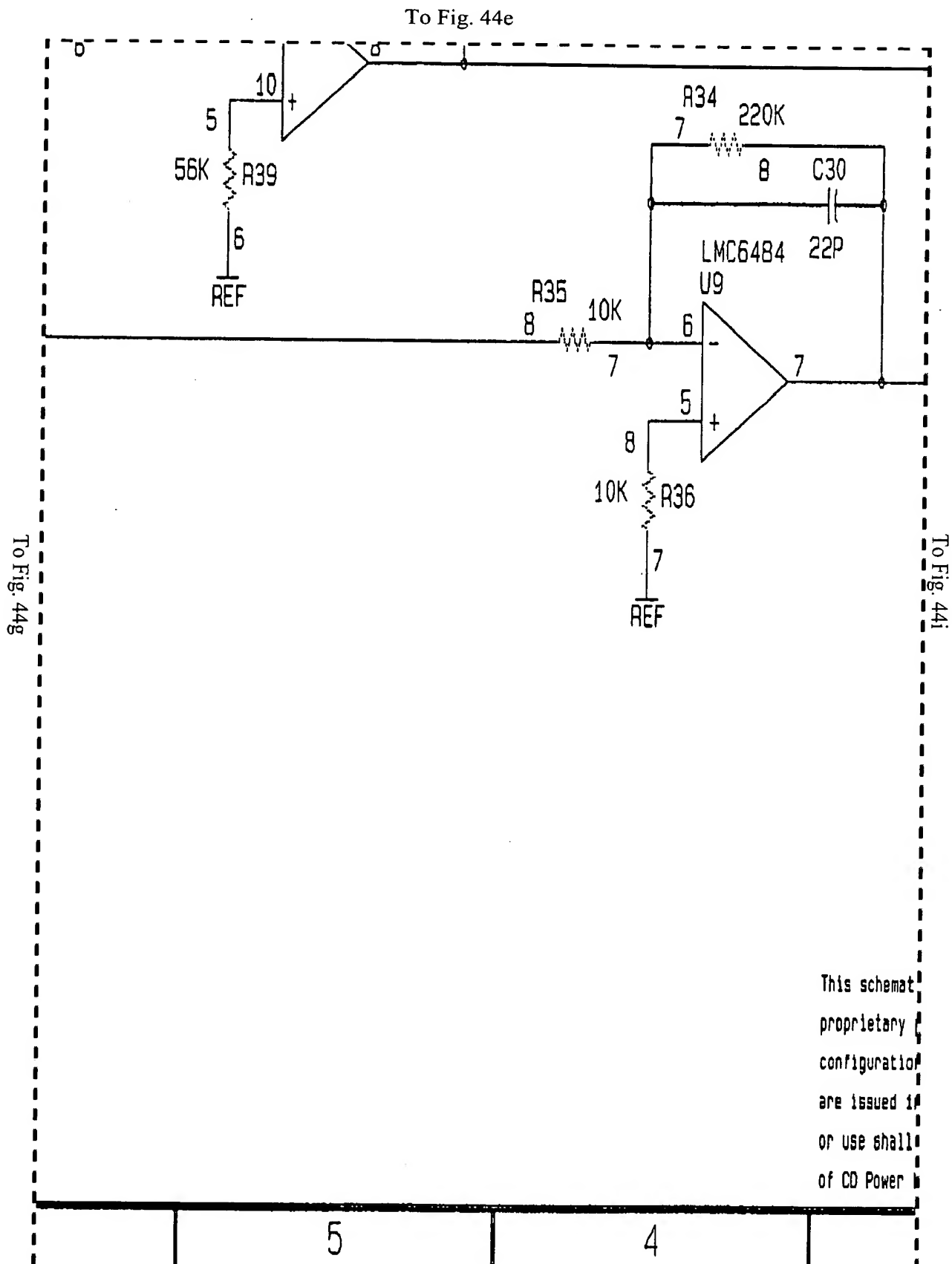
FIG. 44e



The diagram shows a circuit with a thermistor T4 and a resistor R33. The thermistor T4 is connected to a 14-pin connector (I41) and a 15-pin connector (I42). The resistor R33 is connected to the 14-pin connector (I41) and a reference voltage (REF). A diode A16 (1.5KE, 30.0A) is connected to the 15-pin connector (I42) and ground. The circuit is divided into three sections by a dashed line labeled 'ISOLATION'. The left section contains the diode A16 and the thermistor T4. The middle section contains the resistor R33. The right section contains the reference voltage REF. The circuit is labeled with 'I41', 'I42', '14', and '15' at the connector pins. The diagram is labeled 'To Fig. 44h' on the right side.

To Fig. 44h

FIG. 44g



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FIG. 44h

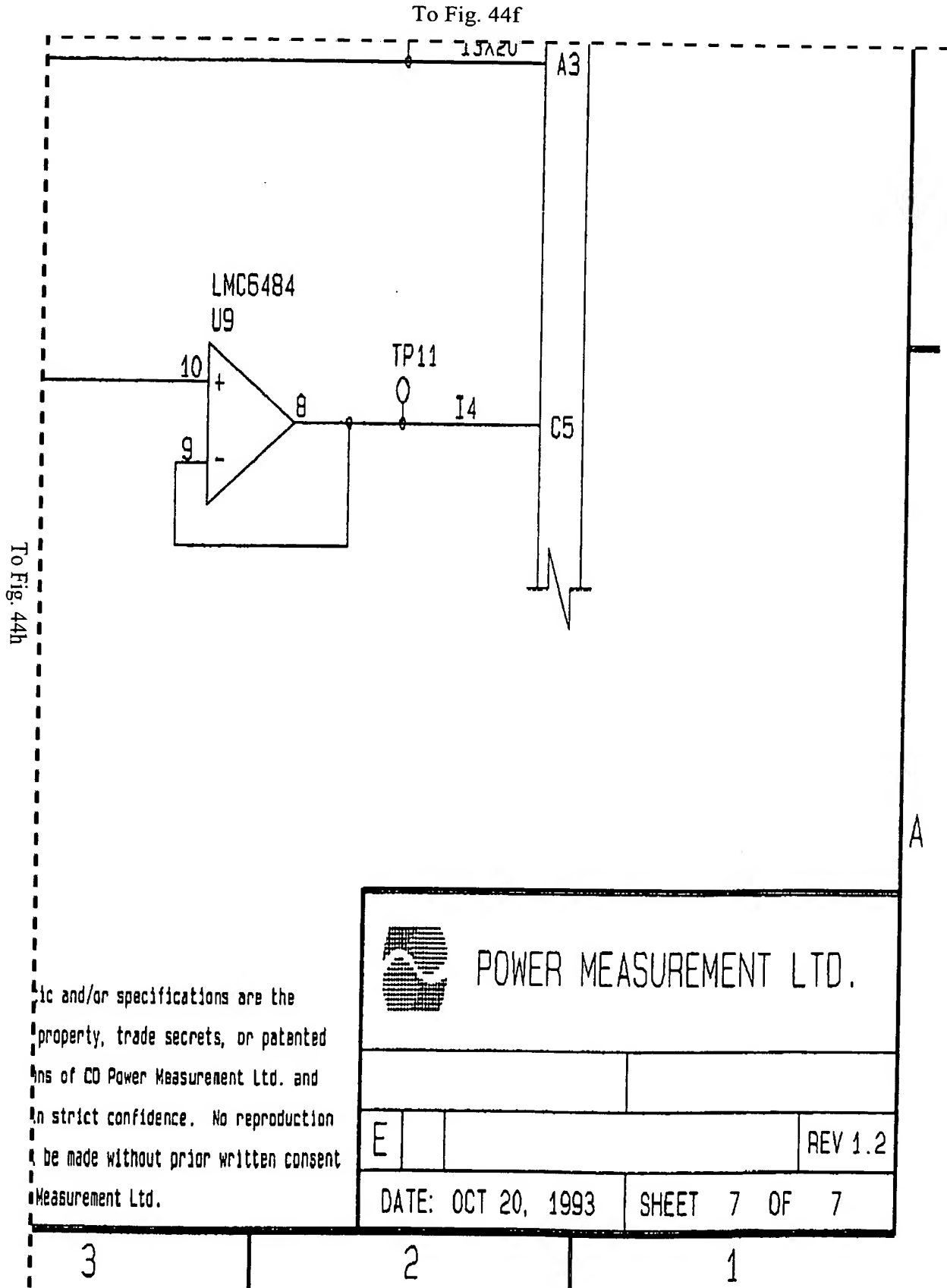
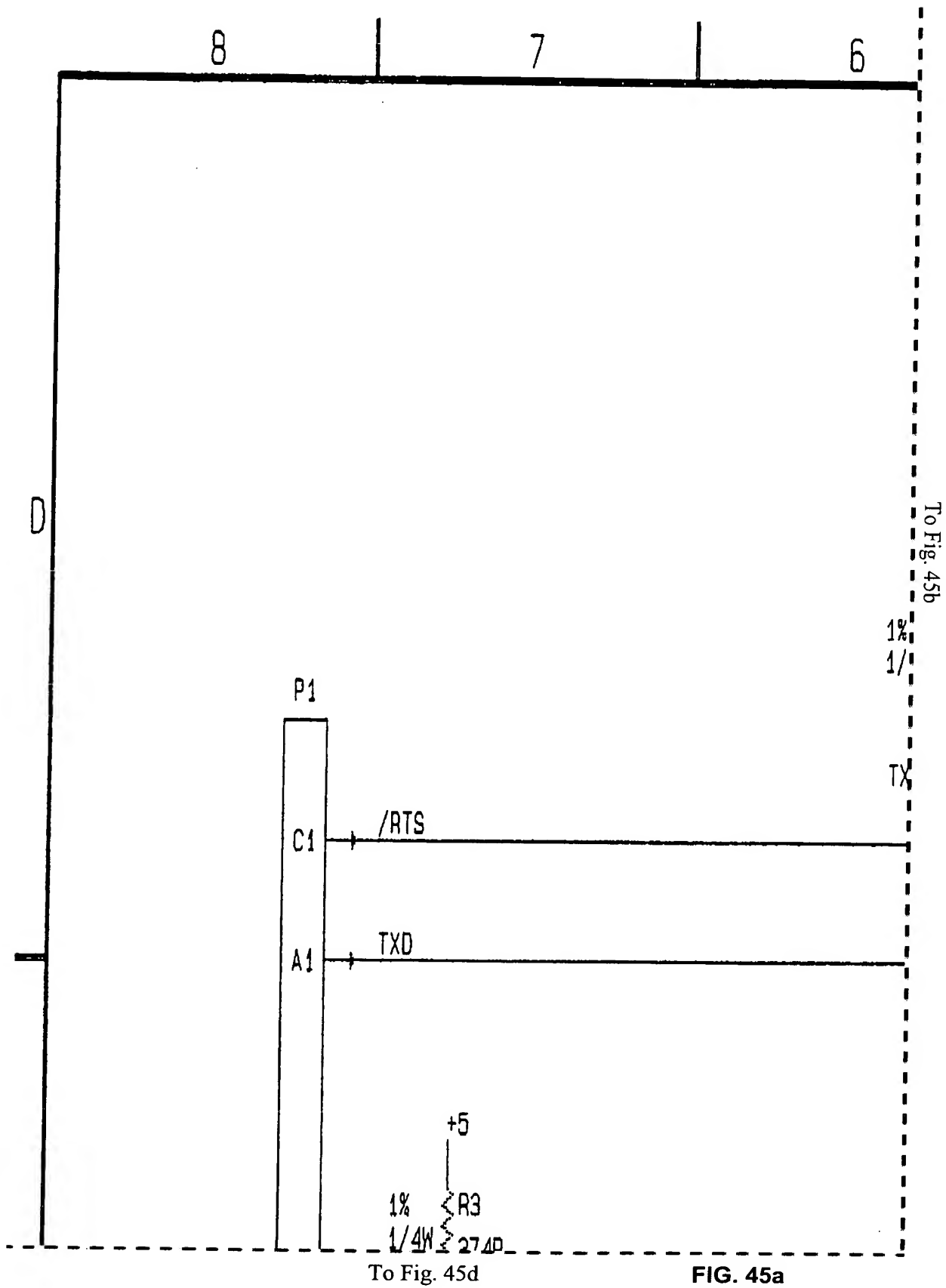


FIG. 44i



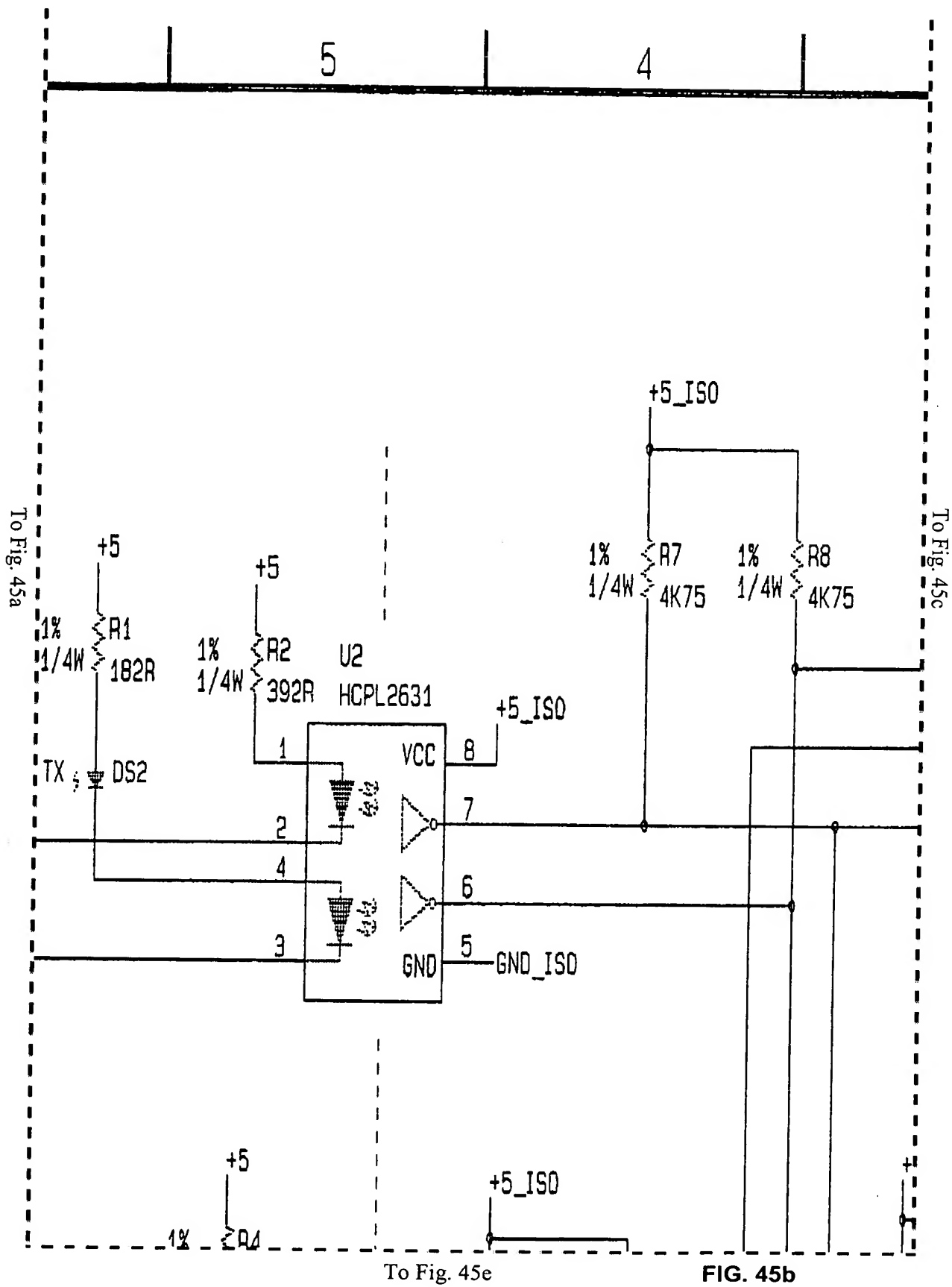


FIG. 45b

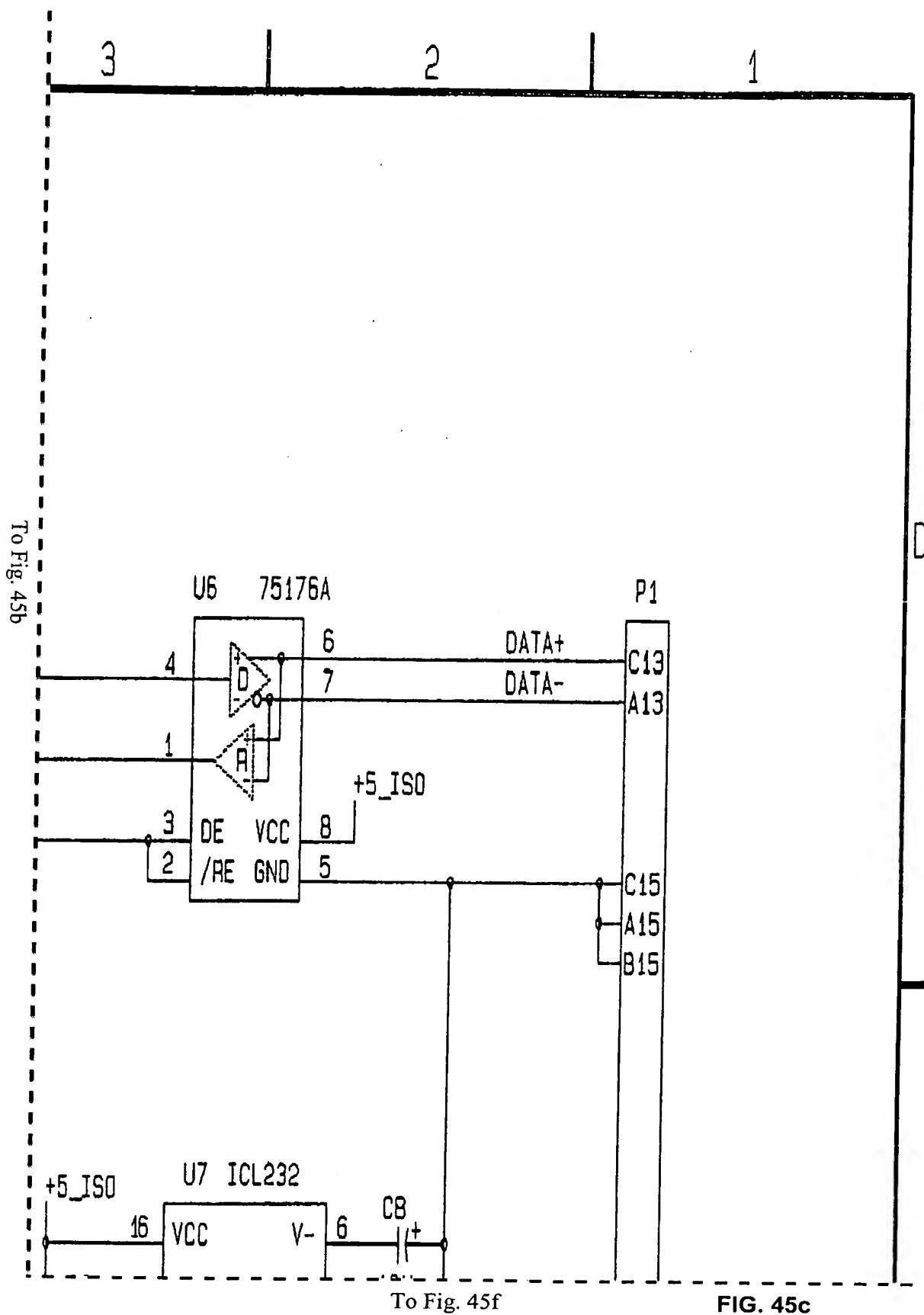
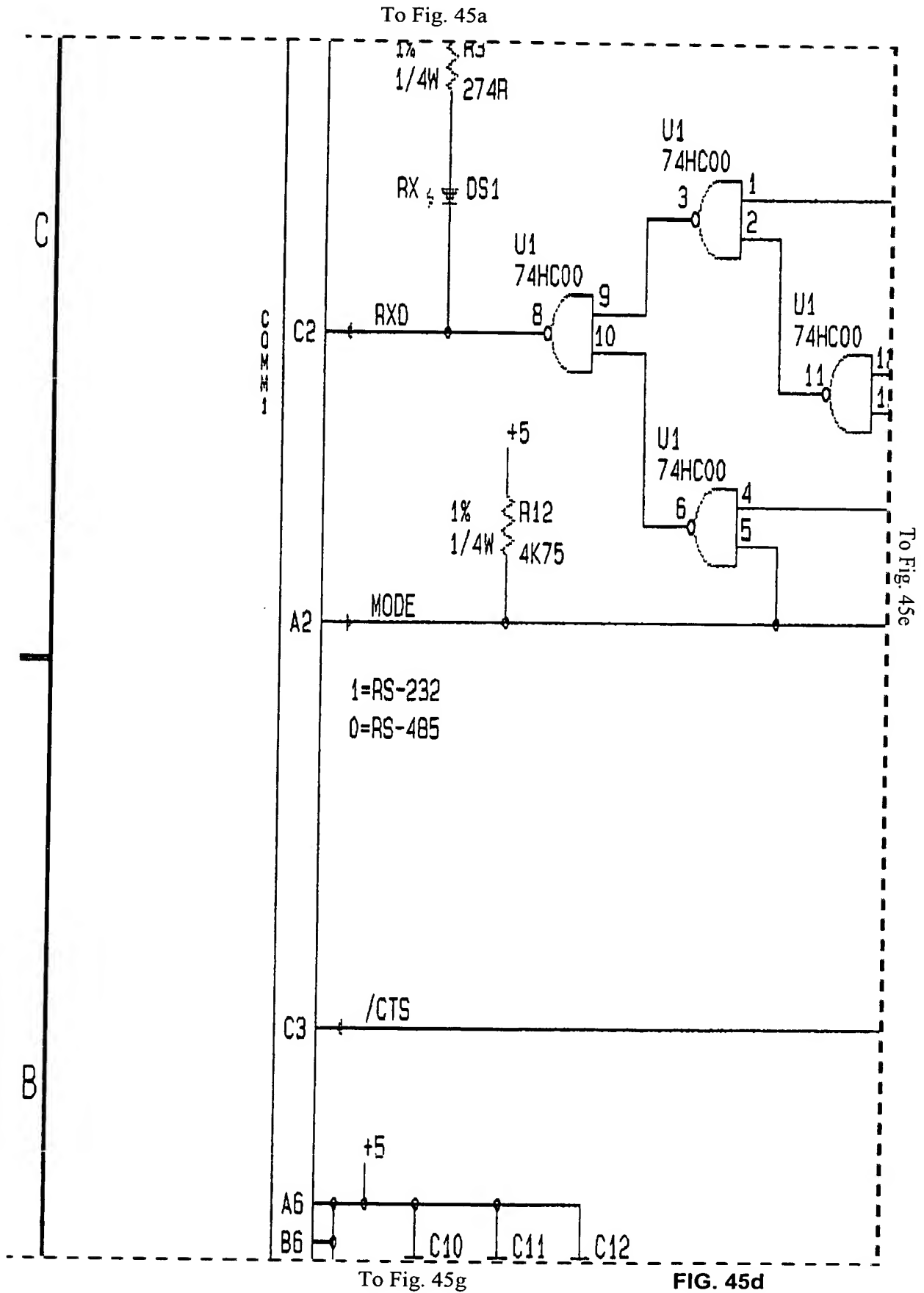
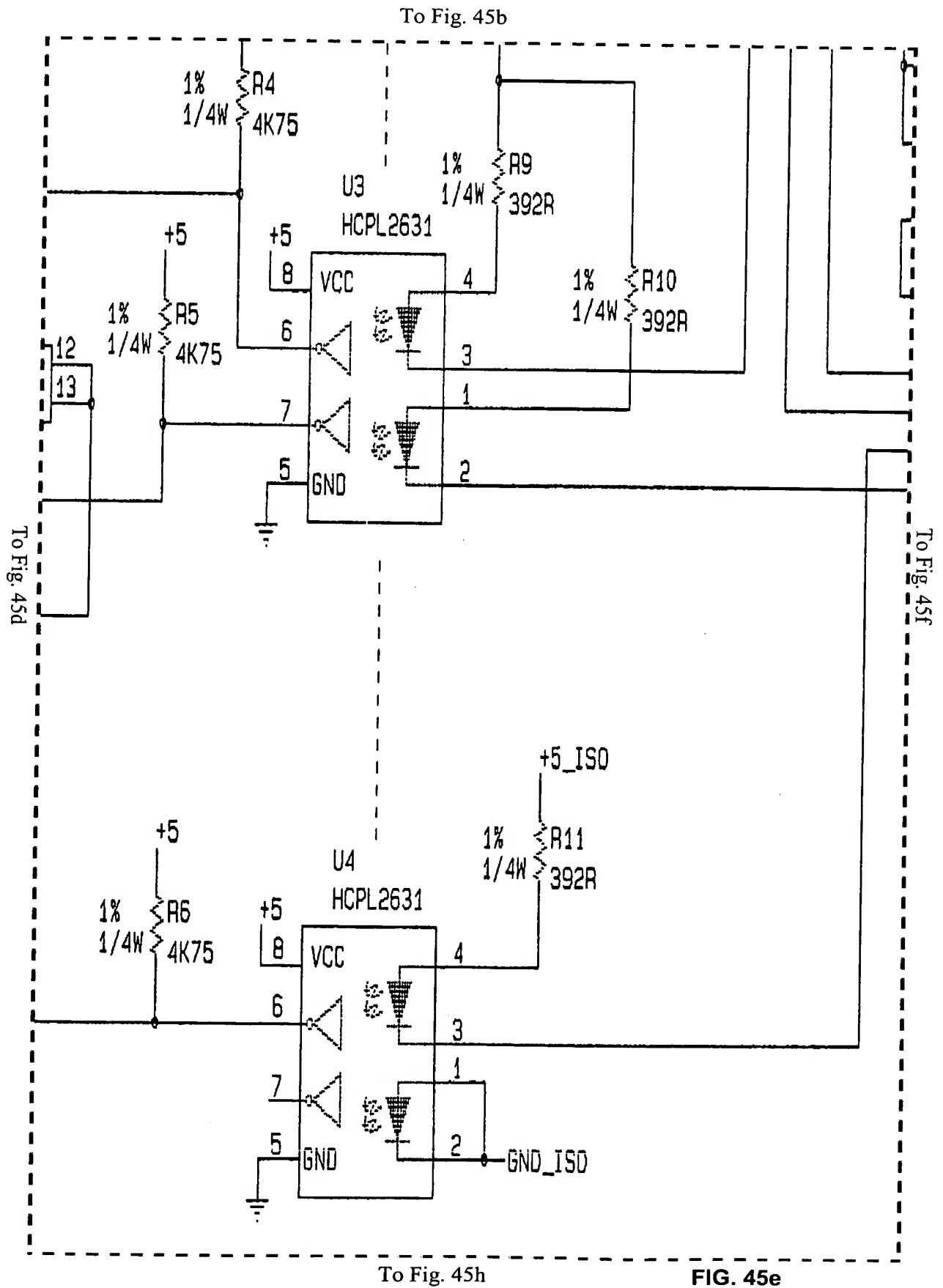
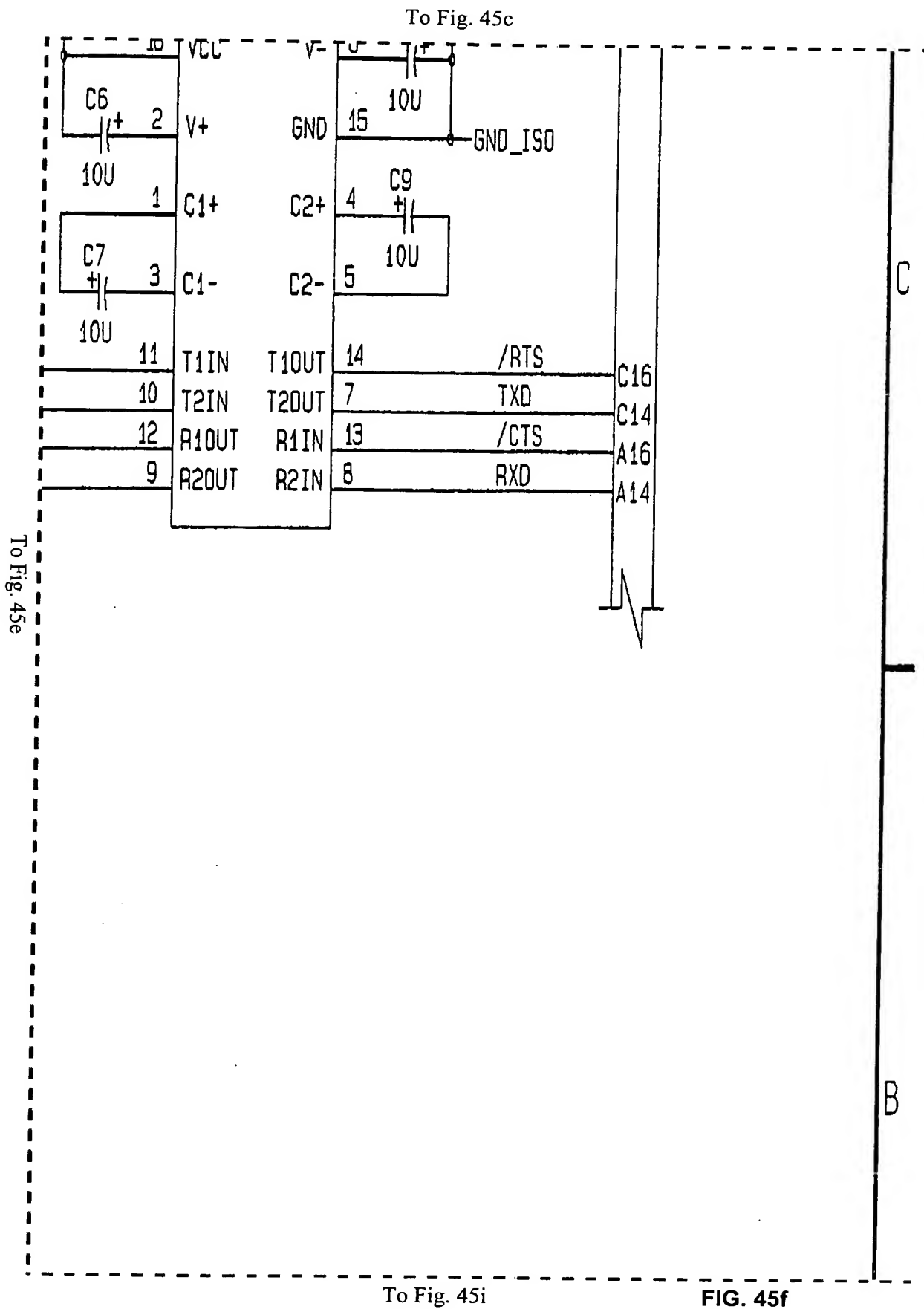


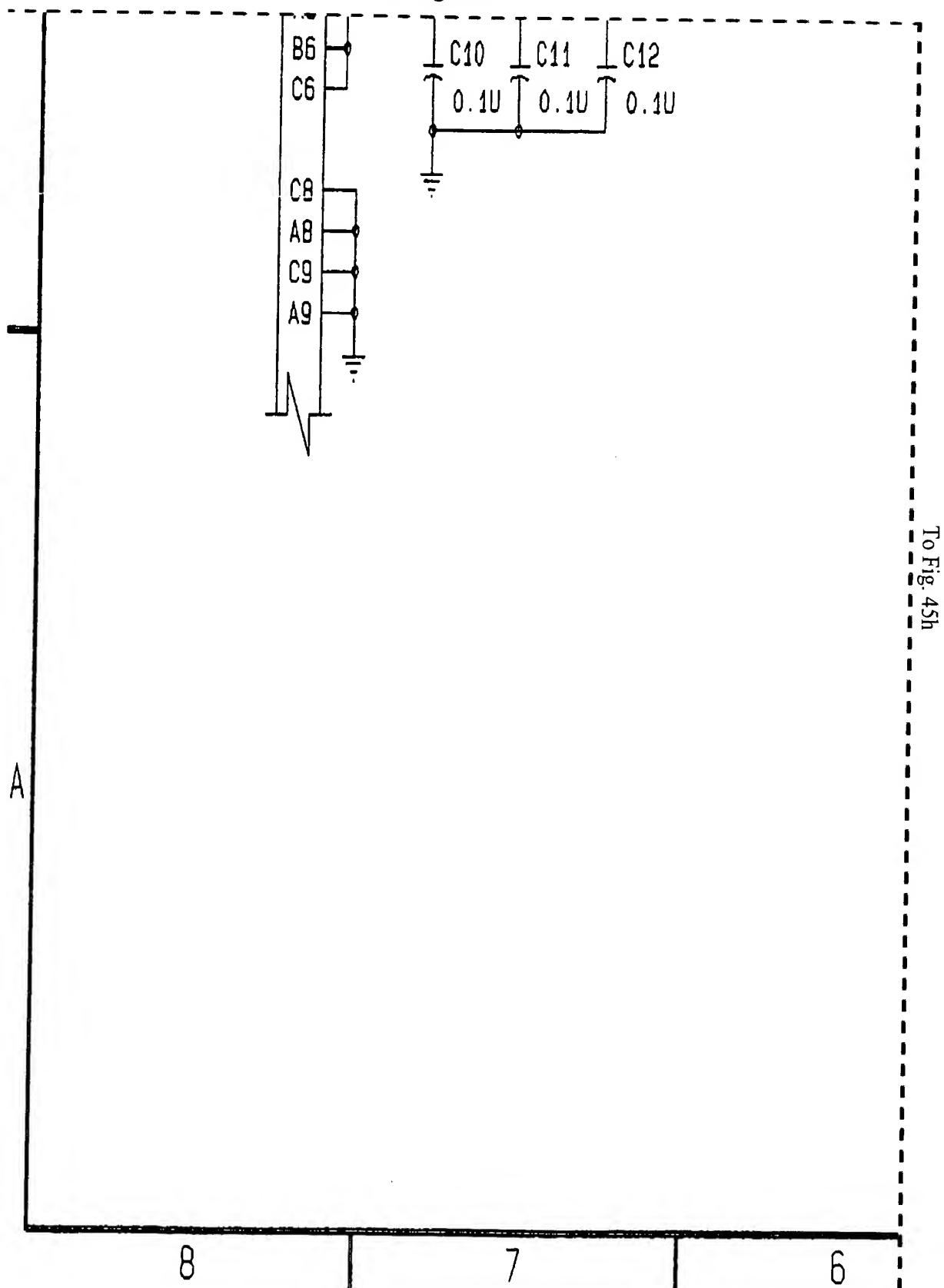
FIG. 45c







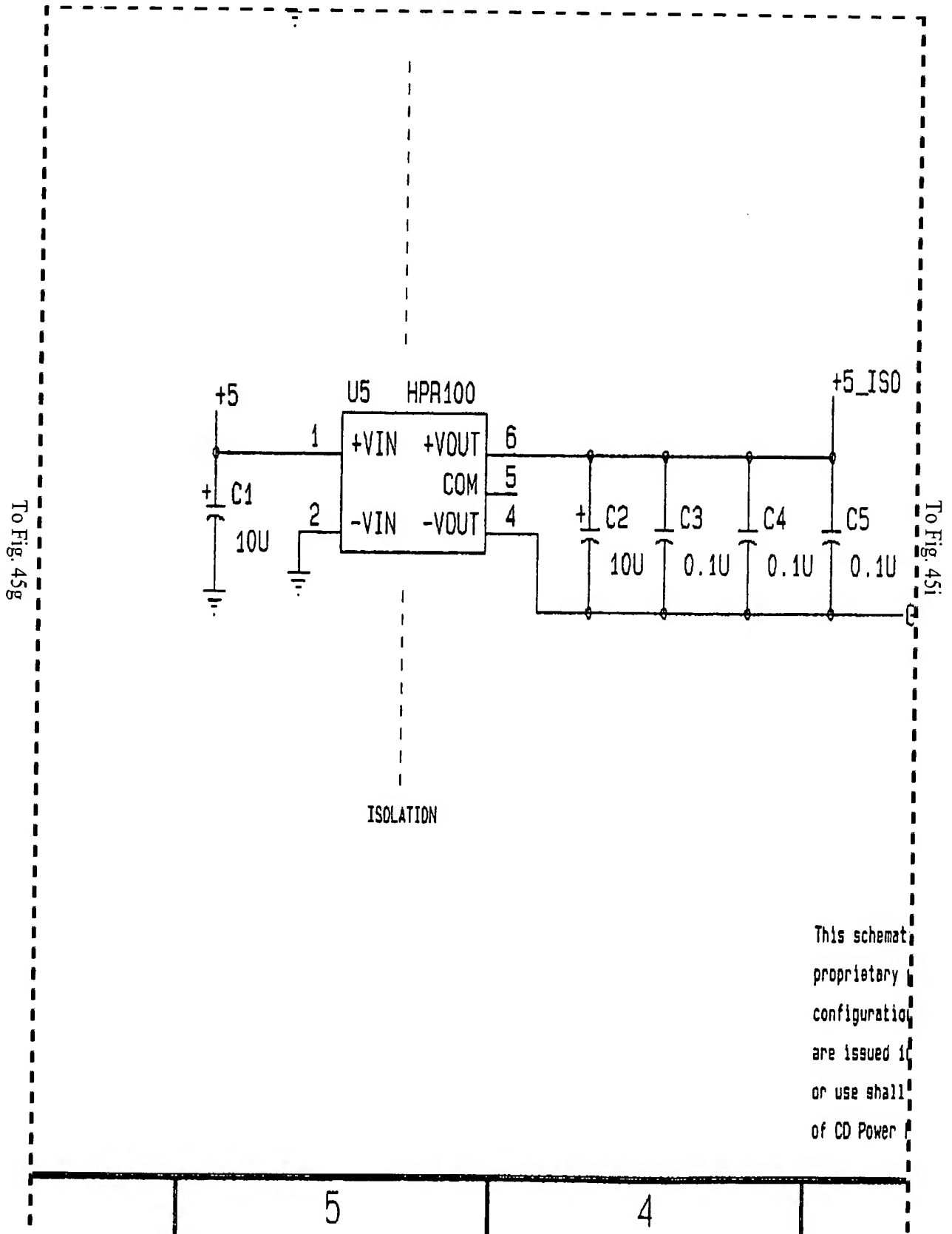
To Fig. 45d



To Fig. 45h

FIG. 45g

To Fig. 45e



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FIG. 45h

To Fig. 45f

To Fig. 45h

GND_ISO

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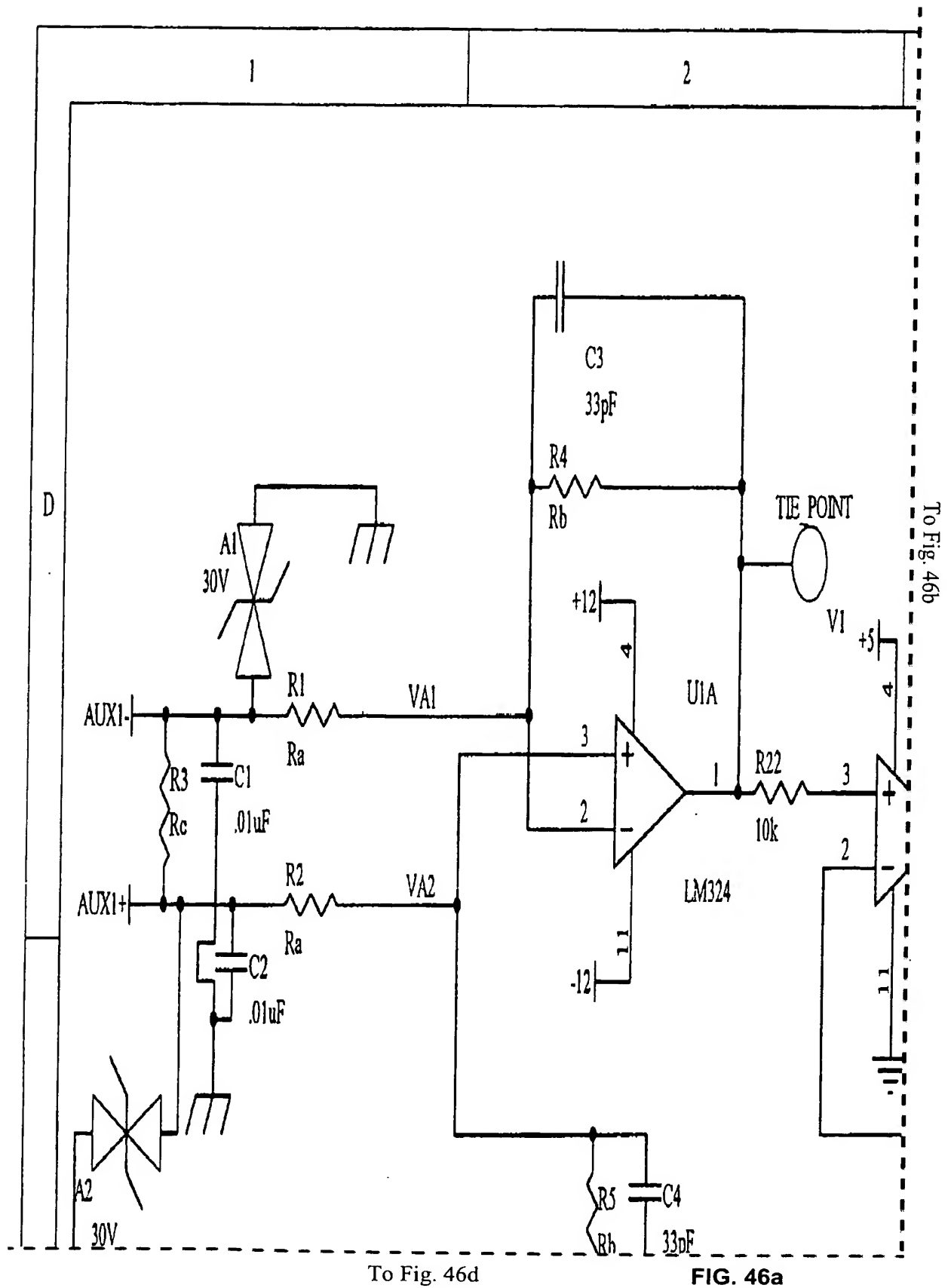
SHEET 1 OF 1

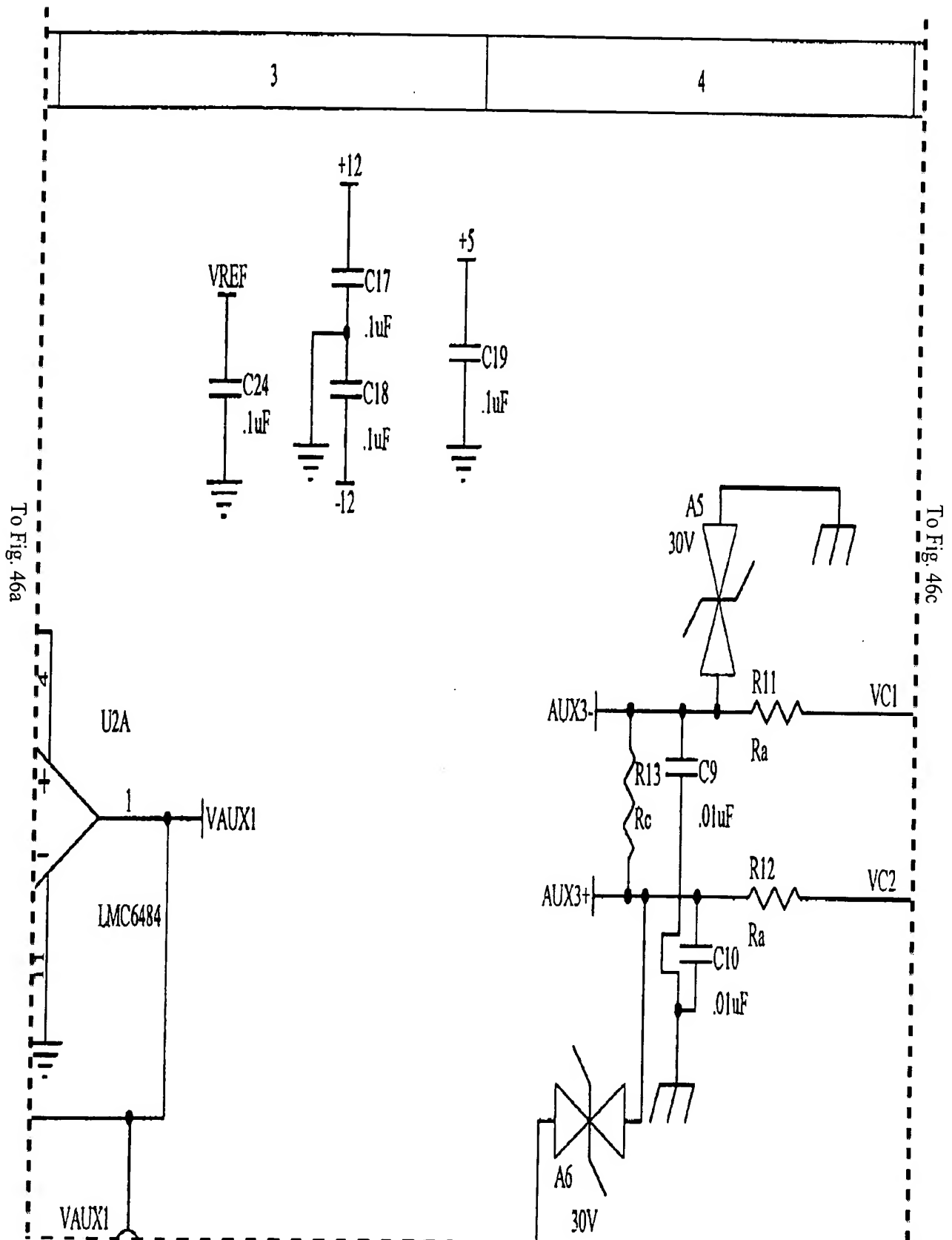
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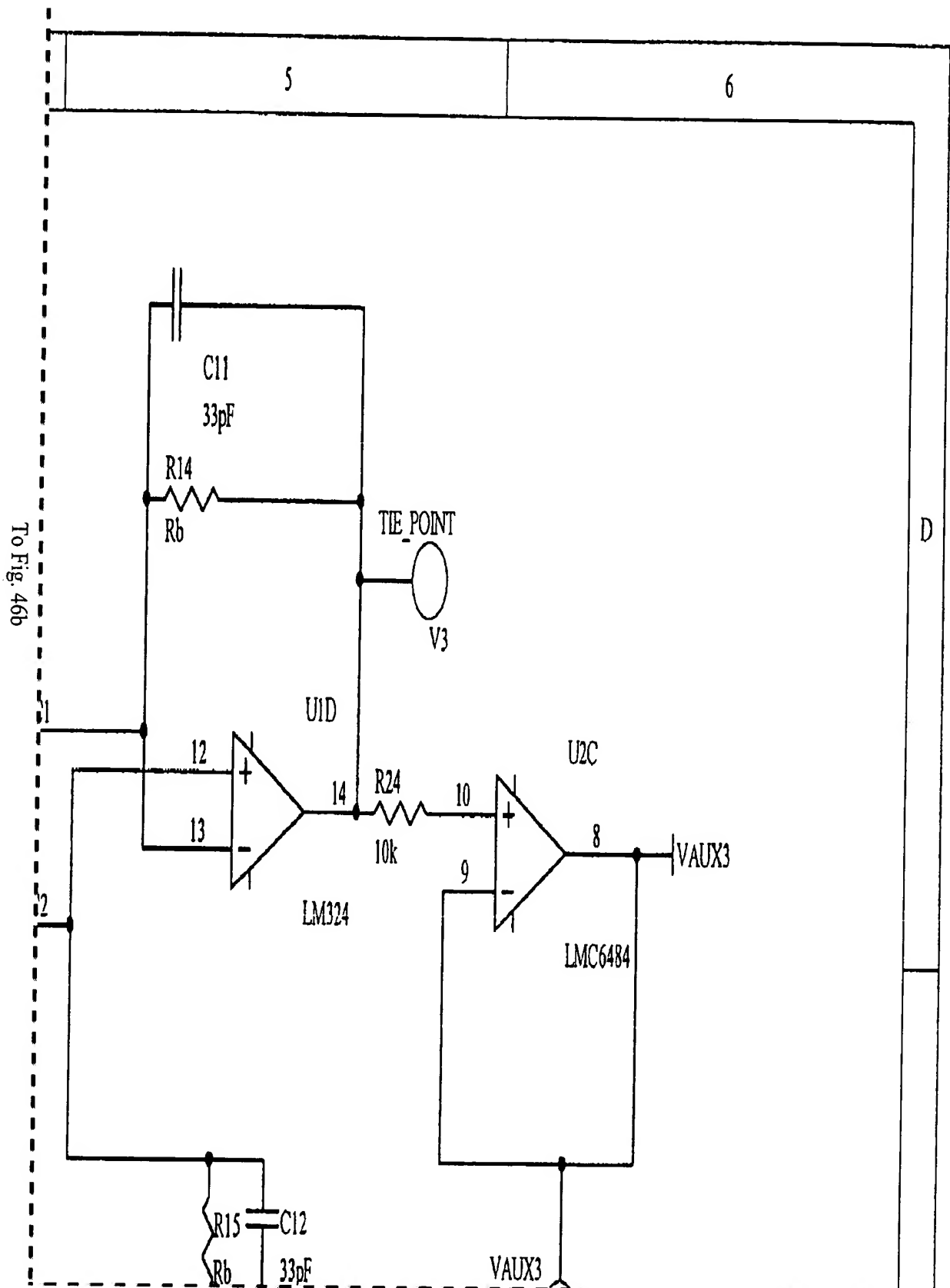
FIG. 45i





To Fig. 46e

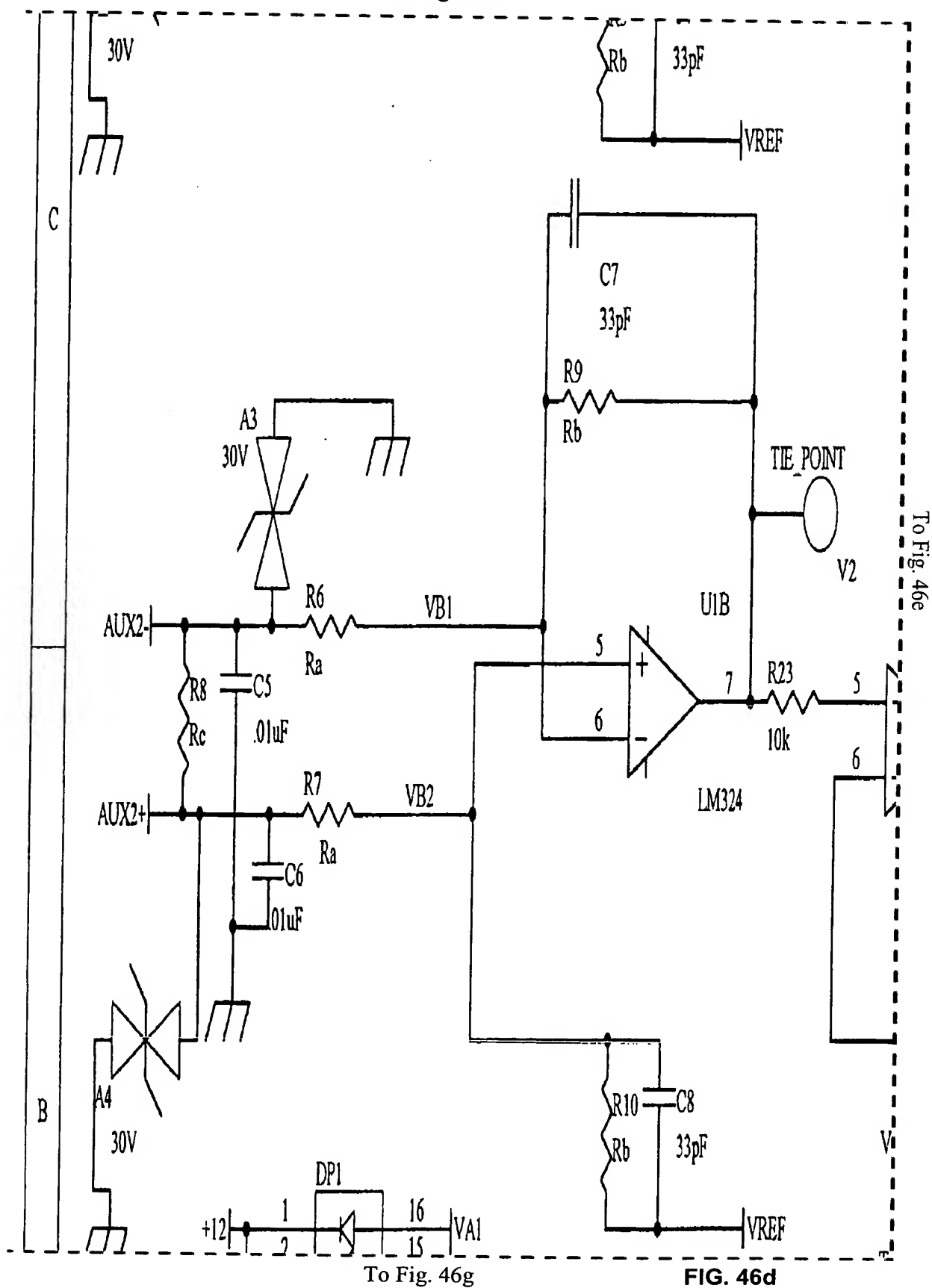
FIG. 46b



To Fig. 46f

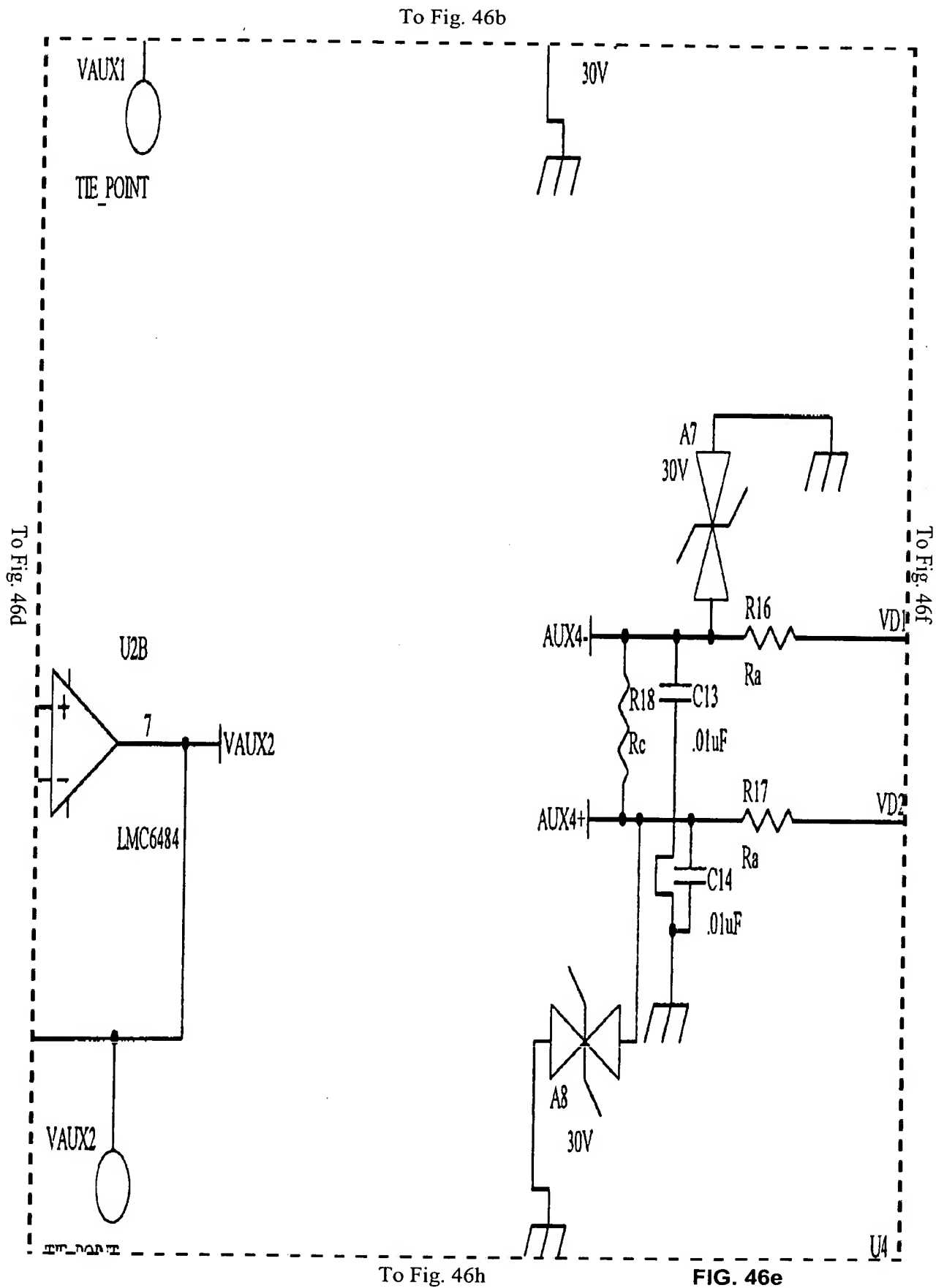
FIG. 46c

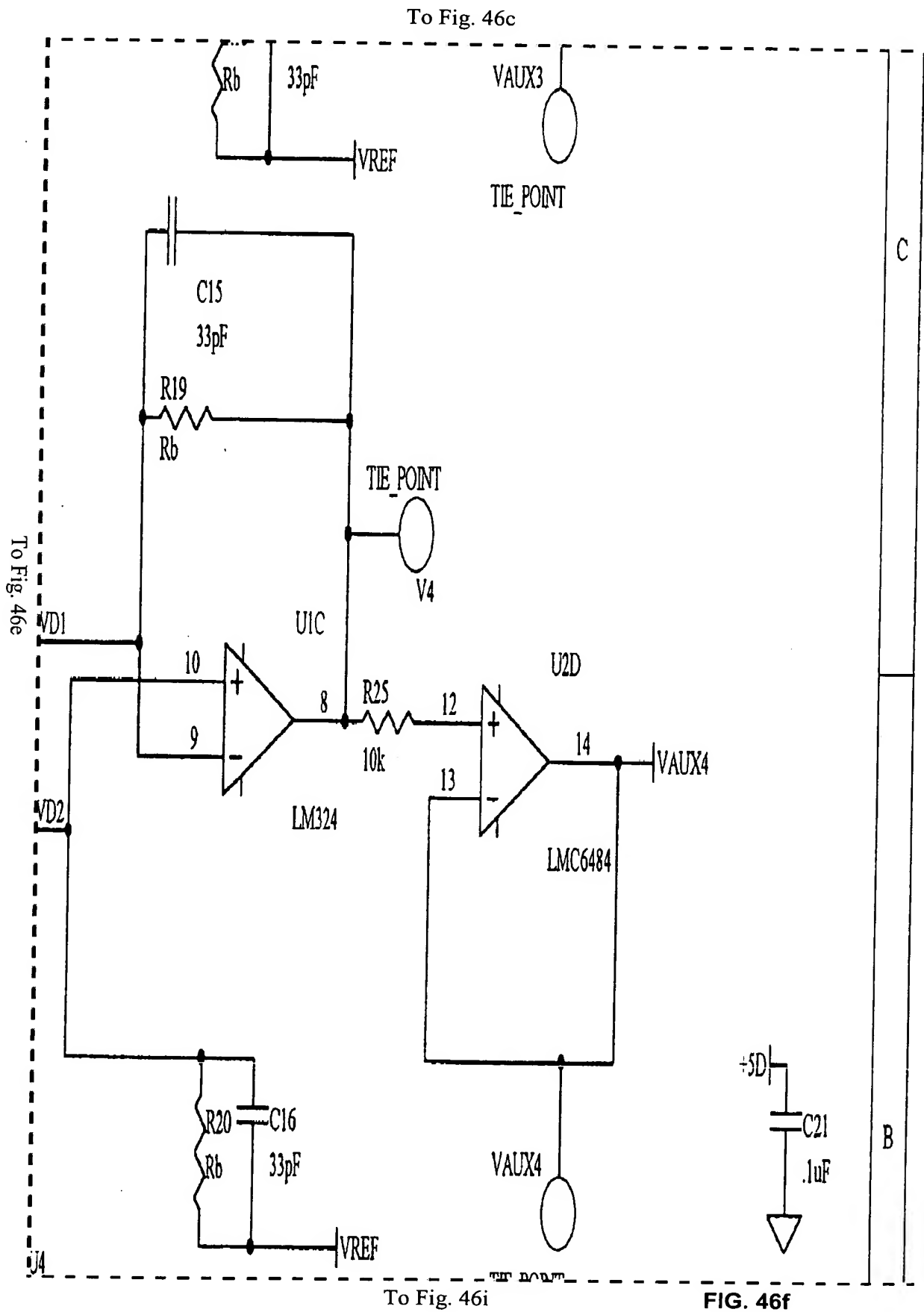
To Fig. 46a



To Fig. 46e

FIG. 46d





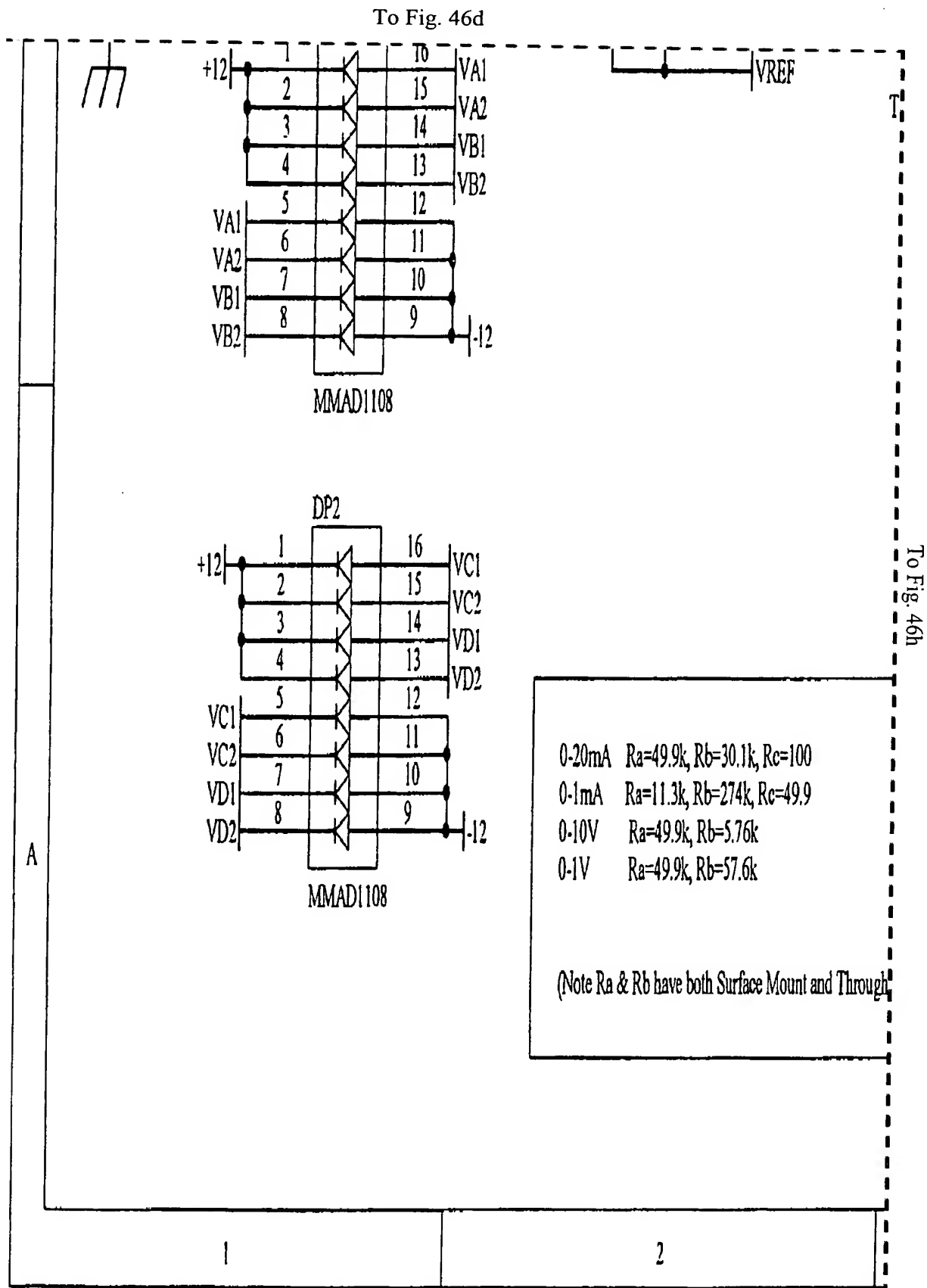
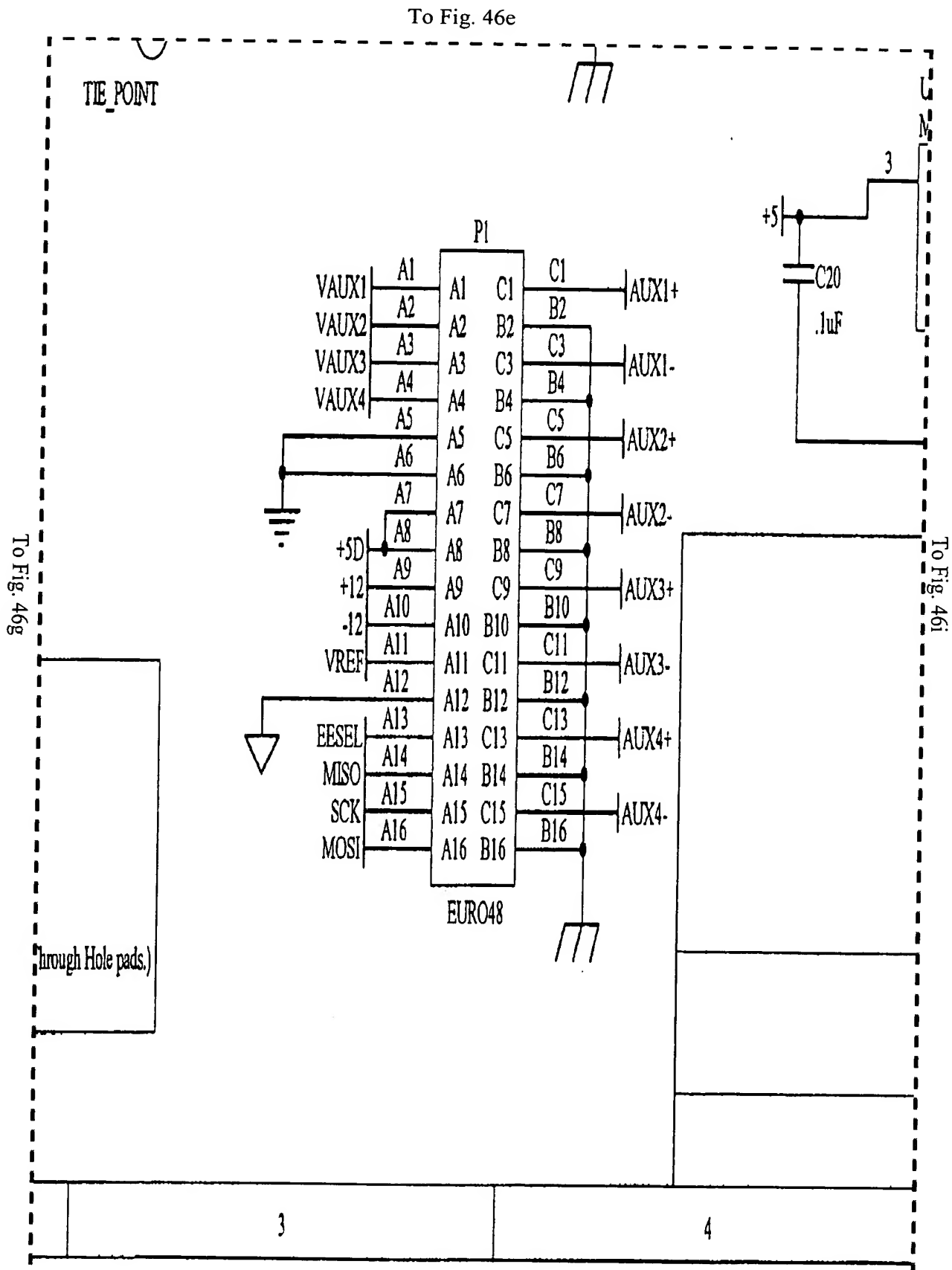
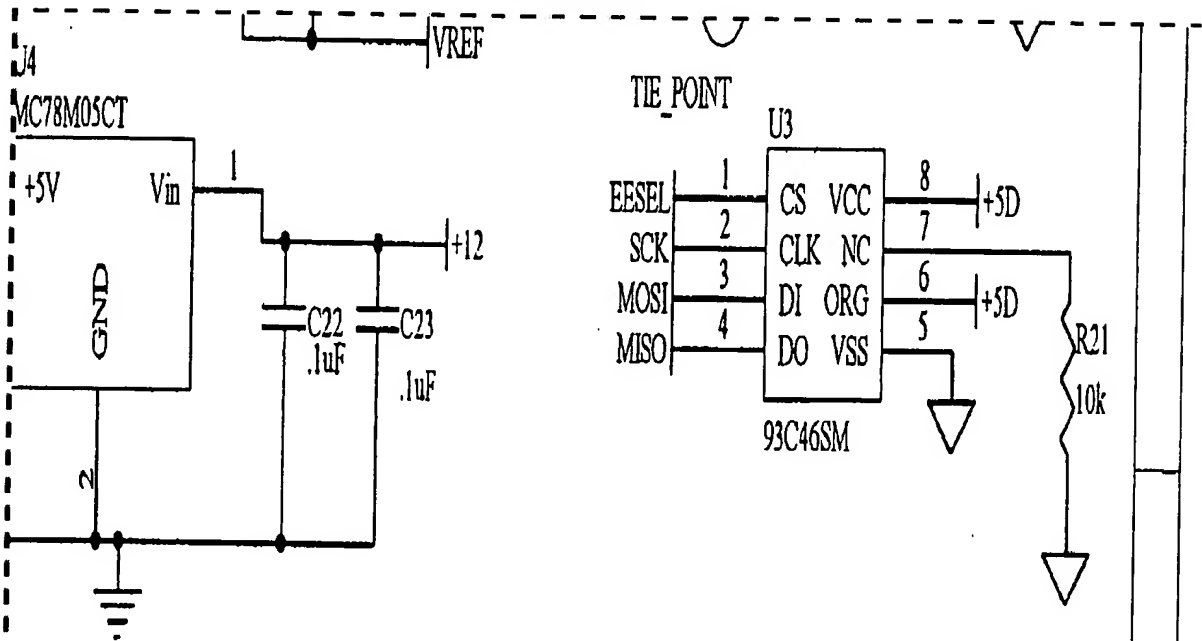


FIG. 46g



To Fig. 46f



To Fig. 46h

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Oct. 19, 1994.

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Sheet
1 of 1

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6

FIG. 46i

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